भारतीय सूचना प्रौद्योगिकी अभिकल्पना एवं विनिर्माण संस्थान , कर्नूल

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY DESIGN AND MANUFACTURING KURNOOL

Jagannathagattu, Kurnool – 518007, Andhra Pradesh, INDIA
(An Institute of National Importance under the Ministry of Education, Govt. of India)

M. Tech. Programme in
Electronic System Design
(With effective from the A.Y. 2020-21)

Scheme, Syllabi and Regulations

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
DESIGN AND MANUFACTURING KURNOOL
KURNOOL-518007, ANDHRA PRADESH, INDIA.
July, 2020

Institute Vision

To become a leading institute of higher learning in Information Technology enabled design & manufacturing to create technologies and technologists befitting the industries globally.

Institute Mission

To become a centre of excellence pioneering in education, research & development, and leaders in design & manufacturing.

Department Vision

To build an academic and research ecosystem with the innovation mindset, for creating industry-ready professionals, entrepreneurs, and researchers in the related fields of Electronics and Communication engineering.

Department Mission

To carry out teaching and research in the areas of Electronics and Communication Engineering, for innovative design and smart manufacturing of the electronic products by the industry and for society at large, by leveraging the innovation in the emerging technologies.

About the programme of M. Tech. in ELECTRONIC SYSTEM DESIGN

Our M. Tech. (ESD) programme is designed to provide advanced theoretical and practical training of all aspects relevant to the design, development, and production of modern electronic systems and subsystems. This programme prepares the students for a wide range of engineering study and career options, including Circuits Design, VLSI, Signal Processing, PCB fabrication, Embedded Systems, and so on.

Curriculum and Syllabus

Department of Electronics and Communication Engineering

Scheme for M. Tech. in **Electronic System Design**

I-Year I-Semester

Sl. No.	Course Code	Course Name	Category Code	I	P	No. of Credits
1	EC501T	Mathematical Foundations for ESD	PEC	3	0	3
2	EC502T	Product Design and Development	DES	3	0	3
3	EC503T	Digital VLSI System Design	PEC	3	0	3
4	EC503I	Embedded System Design Practice	PEC	1	3	3
5	EC502P	Product Design and Development Practice	DES	0	3	2
6	EC503P	Digital VLSI System Design Practice	PEC	0	3	2
7	EC51XT	Elective-I	PEC	3	0	3
8	EC51XT	Elective-II	PEC	3	0	3
9	EC601	Seminar	PCD	--	--	2
Total				**16**	**9**	**24**

I-Year II-Semester

Sl. No.	Course Code	Course Name	Category Code	I	P	No. of Credits
1	EC504T	Circuits for Electronic System Design	PEC	3	0	3
2	EC505T	Electronic Systems Packaging	PEC	3	0	3
3	EC506T	Digital Signal Processing and Architectures	PEC	3	0	3
4	EC504P	Circuits for Electronic System Design Practice	PEC	0	3	2
5	EC505P	Electronic Systems Packaging Practice	PEC	0	3	2
6	EC506P	Digital Signal Processing and Architectures Practice	PEC	0	3	2
7	EC52XT	Elective-III	PEC	3	0	3
8	EC52XT	Elective-IV	PEC	3	0	3
9	EC602	Comprehensive Viva-Voce	PCD	--	--	2
Total				**15**	**9**	**23**

II-Year I-Semester

Sl. No.	Course Code	Course Name	Category Code	I	P	No. of Credits
1	EC604P	Dissertation Work-I	PCD	0	25	10
Total				**0**	**25**	**10**

II-Year II-Semester

Sl. No.	Course Code	Course Name	Category Code	I	P	No. of Credits
1	EC605P	Dissertation Work-II	PCD	0	25	20
Total				**0**	**25**	**20**

LIST OF ELECTIVES

Sl. No.	Course Code	Course Name	Category Code	I	P	No. of Credits
1	EC511	Antenna Design	PEC	3	0	3
2	EC512	Analog and Mixed Signal Circuit Design	PEC	3	0	3
3	EC513	Testing and Testability	PEC	3	0	3
4	EC514	Reliable Digital Communication System Design	PEC	3	0	3
5	EC515	Satellite Communication	PEC	3	0	3
6	EC516	Design of IoT System	PEC	3	0	3
7	EC517	Data Communication and Networking	PEC	3	0	3
8	EC521	Numerical Techniques in Electromagnetics	PEC	3	0	3
9	EC522	RF and Microwave Integrated Circuits	PEC	3	0	3
10	EC523	Electromagnetic Interference and Compatibility	PEC	3	0	3
11	EC524	Software Defined Radio	PEC	3	0	3
12	EC525	Cognitive Communication Networks	PEC	3	0	3
13	EC526	MIMO Communication Systems	PEC	3	0	3
14	EC527	Detection and Estimation Theory	PEC	3	0	3
15	EC528	Electric Vehicle Technology	PEC	3	0	3
16	EC529	Navigation System	PEC	3	0	3

Semester-I Courses

Course Title	Course Code	Structure (I-P-C)		
Mathematical Foundations of ESD	**EC501T**	**3**	**0**	**3**

Pre-requisite, if any: Nil

Course Outcomes: At the end of the course, the students will be able to:

CO1	Simulate appropriate application/distribution problems.
CO2	Obtain the value of the point estimators using the method of moments and method of maximum likelihood.
CO3	Apply the concept of various test statistics used in hypothesis testing for mean and variances of large and small samples.
CO4	Get exposure to the principal component analysis of random vectors and matrices.
CO5	Analyse the time complexity of the operation of the digital operations.
CO6	Apply Galois Field theory in the cryptography applications.

Syllabus:

SPECIAL FUNCTIONS: Bessel's equation – Bessel function – Recurrence relations - Generating function and orthogonal property for Bessel functions of first kind – Fourier-Bessel expansion.

LINEAR PROGRAMMING: Formulation – Graphical solution – Simplex method – Two phase method –Transportation and Assignment Problems.

SIMULATION: Discrete Event Simulation – Monte – Carlo Simulation – Stochastic Simulation – Applications to real time problems.

ESTIMATION THEORY: Estimators: Unbiasedness, Consistency, Efficiency and Sufficiency – Maximum Likelihood Estimation – Method of moments.

MULTIVARIATE ANALYSIS: Random vectors and Matrices – Mean vectors and Covariance matrices – Multivariate Normal density and its properties – Principal components: Population principal components – Principal components from standardized variables.

COMPLEXITY ANALYSIS: Introduction to time complexity of an algorithm or operation (worst case, average case, and best case), SAT problems, NP hard and NP complete problems.

ABSTRACT ALGEBRA: Introduction to Group, Ring, and Fields, Prime/Polynomial field representation, Irreducible polynomial, primitive polynomial, minimal polynomial, Galois field (GF) addition, GF multiplication, GF exponentiation, and GF multiplicative inverse.

Text Book(s):

1. Jay L. Devore, “Probability and Statistics for Engineering and the Sciences”, Cengage Learning, 9th Edition, Boston, 2016.
2. Erwin Kreyszig. “Advanced Engineering Mathematics”, John Wiley & Sons, 10th Edition, New York, 2010.

References & Web Resources:

1. Johnson, R.A, Irwin Miller and John Freund., "Miller and Freund's Probability and Statistics for Engineers", Pearson Education, 9th Edition, New York, 2016.
2. Johnson, R.A., and Wichern, D.W., "Applied Multivariate Statistical Analysis", Pearson Education, Sixth Edition, New Delhi, 2013.
3. Ross. S.M., "Probability Models for Computer Science", Academic Press, SanDiego, 2002.
4. Taha H.A. "Operations Research: An Introduction", Prentice Hall of India Pvt. Ltd. 10th Edition, New Delhi, 2017.
5. Winston, W.L., "Operations Research", Thomson – Brooks/Cole, Fourth Edition, Belmont, 2003.
6. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, Clifford Stein, "Introduction to Algorithms", MIT Press, 2009.
7. Ralph P. Grimaldi, "Discrete and combinatorial Mathematics", Pearson Education, 5th Edition, New Jersey, 2004.

Course Title	Course Code	Structure (I-P-C)		
Product Design and Development	**EC502T**	**3**	**0**	**3**

Pre-requisite, if any: Nil

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the systematic approach used during product design and development.
CO2	Learn the methods for need identification, techniques for creative thinking, concept generation, concept selection, product architecture, aesthetics, ergonomics etc.
CO3	Visualize the concepts using models and realize the design models using suitable materials
CO4	Understand the needs of a customer and use creative thinking to conceptualize designs.

Syllabus:

Introduction: Importance of engineering design, types of design, total life cycle- types of products, Phases of product development process, product and process cycles.

Problem Definition & Need Identification: Identifying customer needs, gathering information classifying customer requirements, engineering characteristics, competitive benchmarking, QFD, product design specification.

Conceptual Design: Creativity in design, creativity and problem solving, creative thinking methods, conceptual decomposition morphological methods-TRIZ and contradiction, Bio and Shape mimicry techniques, Decision making and concept selection decision theories-concept screening and scoring.

Embodiment Design: Product architecture, steps in developing product architecture, industrial design human factors design, Nostalgia and Design, Environment factors.

Design Profile Preparation

Text Book(s):

1. K. Otto, Product Design, Pearson Education, 1st edition, 2011, ISBN: 8177588214.
2. U. Karl and S. Eppinger, Product Design and Development, McGraw-Hill Education, 5th edition, 2012, ISBN: 0073404772.

References & Web Resources:

1. C. A. Harper, Handbook of Materials for Product Design, McGraw-Hill Professional, 1st edition, 2001, ISBN: 0071354069.
2. R. Stuer and K. Eissen, Sketching: Drawing Techniques for Product Designers, Thames & Hudson, 1st edition, 2007, ISBN: 9063691718.
3. B. Hallgrimsson, Prototyping and Modelmaking for Product Design, Laurence King Publishing, 1st edition, 2012, ISBN: 9781856698764

Course Title	Course Code	Structure (I-P-C)		
Digital VLSI System Design	**EC503T**	**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Design, VLSI Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design digital system using Verilog HDL and CMOS transistors..
CO2	Analyse the circuit/system performance, area, and power dissipation.
CO3	Implement the low power and high throughput techniques on analog, digital, and mixed signal integrated circuits.
CO4	Develop the Custom IPs to integrate into Digital Systems using Xilinx Vivado.

Syllabus:

Introduction to Digital design: timing issues, pipelining, folding/unfolding, resource sharing, metastability, synchronization, clock skew, setup/hold time of flip-flops, synchronization between multiple clock domains using FIFO, PLL, and DLL, reset – recovery/removal time, false path.

Digital Systems Design with ASICs: PLDs, Semi/full custom ASIC designs, Emphasis on the synthesis based approach to VLSI Design. Relevant issues related to physical design automation such as partitioning, floor planning, power planning, placement & routing, Algorithms for VLSI Physical Design, IO pads, electro static discharge.

Digital Systems Design with FPGAs: Hardware-Software Co-design, Custom IP development, High level synthesis (HLS), Efficient Coding Techniques in High Level Language for HLS, Partial Reconfiguration.

Hardware Verification and Testing Equivalence/model check based formal hardware verification, Binary decision/moment diagram, flexible/vector hardware designs, VLSI testing, logical fault models, fault equivalence, fault dominance, fault collapsing, double/triple

modular redundancy, fault simulation, test pattern generation, Built-in-self test, Scan chain based test, fault tolerant designs.

CMOS Transistor Logic: I-V characteristics, Short channel effects, Mobility degradation & velocity saturation, channel length modulation, body effect, drain induced barrier lowering, leakage, RC delay model, logical effort, clock gating, dynamic voltage scaling, power gating, glitch free circuits, dual-edge triggering, static CMOS, ratioed circuits, dynamic CMOS, domino logic, pass transistor logic, CMOS latches, CMOS flip flops, dual edge triggered flip flops, synchronizers, arbiters, wave pipelining.

Text Book(s):

1. Neil H.E. Westte and David Money Harris: CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley, 4th Edn, 2011.

References & Web Resources:

1. Wakerly, J. F., Digital Design: Principles and Practices, 4th Edition, Pearson, 2008
2. Miron Abramovici, Melvin A Breuer, and Arthur D Friedman: Digital Systems Testing and Testable Designs, Wiley-IEEE Press, 1994.
3. N. A. Sherwani, Algorithms for VLSI Physical Design Automation, Bsp Books Pvt. Ltd., 3rd edition, 2005.
4. Samir Palnitkar: Verilog HDL - Guide to Digital design and synthesis, Pearson Education, 3rd Edn, 2003.

Course Title	Course Code	Structure (I-P-C)		
Embedded System Design Practice	**EC503I**	**1**	**3**	**3**

Pre-requisite, if any: Microprocessors and Microcontrollers

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the basic elements of embedded systems such as I/O and interfaces.
CO2	Understand embedded system design using the ARM Cortex-M microcontroller with the Launchpad IDE in C.
CO3	Develop the rapid prototype of embedded systems using open source microcontrollers and microcomputers such as Arduino, Raspberry Pi, BeagleBone Black, and Intel Edison/Galileo
CO4	Build wireless networked embedded systems using Arduino shields and modules (e.g., GPS, GSM/GPRS, Bluetooth, RFID, and ZigBee).
CO5	Exploit the advanced concepts such as networking and wireless communications, real-time operating systems and control, and Internet of Things in the real time embedded systems.
CO6	Develop the hardware-software co-design with parallel threads using Xilinx Vivado, and Conduct experiments in Internet of Things (e.g., using Arduino Yun, Intel and Microsoft Developer Kits)

Syllabus:

Elements of embedded systems (such as microcontrollers, GPIO, communication, interrupts, ADC, and DAC); overview of microcontroller; Comparison between Hardware, Software, and Firmware; Comparison between Hard, Soft, Firm, and Hybrid real time systems; applications of embedded systems; classification of embedded systems; characteristics of embedded systems; hardware-software partitioning;
Software aspects of embedded systems; Real-time operating system (RTOS) - mutual exclusion; deadlock; critical section; event-driven scheduling; time sharing; earliest deadline first scheduling; pre-emptive scheduling; non-pre-emptive scheduling; multi-tasking; multi-threading; inter-process communication using semaphores, mboxes, and pipes; priority inversion;
Rapid prototyping of embedded systems with advanced microcontroller boards; Basic elements of IoT; IoT systems design using advanced microcontroller boards.

Detailed Syllabus for Lab Practice

1. Experiments in GPIO such as switches, LEDs, LCD, Key pad, Seven Segment Display, Buzzer, and relay;

2. Serial and parallel interfacing; data acquisition with ADC, audio, and video; timer interrupts; various bus interconnects such as I2C, UART, SPI, and so on;

3. DAC Experiments in control of RC servos, stepper motors, and DC motors;

4. Data acquisition and real-time control with TIVA boards, LPC2148 trainer board, FPGA boards, Arduino, Raspberry Pi, and BeagleBone Black microcontrollers;

5. Add-on boards Experiments in wireless networked systems with GPS, GSM/GPRS, ZigBee, Bluetooth, and RFID;

6. Hardware-software co-design experiments using FPGA boards.

7. Experiments in IoT for smart automation using sensors, microcontrollers, and cloud.

8. Free RTOS based applications using TIVA board.

Text Book(s):

1. J. W. Valavano, Embedded Systems: Introduction to Arm Cortex-M Microcontrollers, 2nd edition, Create Space, 2012. ISBN: 978-1477508992.
2. J. W. Valavano, Embedded Systems (Vol-2): Real-Time Interfacing to ARM Cortex-M Microcontrollers, 2nd edition, Create Space, 2011, ISBN: 978-1463590154.

References & Web Resources:

1. J. W. Valavano, Embedded Systems (Vol-3): Real-Time Operating Systems for Arm Cortex M Microcontrollers, 2nd edition, Create Space, 2012. ISBN: 978-1466468863.
2. A. McEwen and H. Cassimally, Designing the Internet of Things, 1st edition, Wiley, 2013. ISBN: 978-8126556861.
3. D. Gajski, F. Vahid, S. Narayan, and J. Gong. Specification and Design of Embedded Systems, Prentice Hall.

Course Title	Course Code	Structure (I-P-C)		
Product Design and Development Practice	**EC502P**	**0**	**3**	**2**

Pre-requisite, if any: Nil

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the systematic approach used during product design and development.
CO2	Learn the methods for need identification, techniques for creative thinking, concept generation, concept selection, product architecture, aesthetics, ergonomics etc.
CO3	Visualize the concepts using models and realize the design models using suitable materials
CO4	Understand the need of a customer and use creative thinking to conceptualize designs.
CO5	Understand the systematic approach used during product design and development.

Syllabus:

Method of Expressing and communicating and documenting technical ideas through sketches.

Clay, Foam, Wood modelling and modern 3D printing.

Problem Definition and Need Identification.

Conceptual design: Morphological charts, TRIZ and Contradiction, Bio and Shape mimicry, Concept selection, Screening.

Embodiment Design: Product Architecture, Human Factors, Aesthetics, Nostalgia and Environmental factors.

Design Profile presentation.

Text Book(s):

1. K. Otto, Product Design, Pearson Education, 1st edition, 2011, ISBN: 8177588214.
2. U. Karl and S. Eppinger, Product Design and Development, McGraw-Hill Education, 5th edition, 2012, ISBN: 0073404772.

References & Web Resources:

1. C. A. Harper, Handbook of Materials for Product Design, McGraw-Hill Professional, 1st edition, 2001, ISBN: 0071354069.
2. R. Stuer and K. Eissen, Sketching: Drawing Techniques for 6|P a g e Product Designers, Thames & Hudson, 1st edition, 2007, ISBN: 9063691718.
3. B. Hallgrimsson, Prototyping and Modelmaking for Product Design, Laurence King Publishing, 1st edition, 2012, ISBN: 9781856698764.

Course Title	Course Code	Structure (I-P-C)		
Digital VLSI System Design Practice	**EC503P**	**0**	**3**	**2**

Pre-requisite, if any: Digital Logic Design, VLSI Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design digital system using Verilog HDL and CMOS transistors
CO2	Develop the hardware-software co-design using Xilinx Vivado.
CO3	Develop the custom IP using RTL design and/or high level synthesis with Xilinx Vivado
CO4	Design the digital system with low power and high throughput VLSI techniques
CO5	Implement the fault tolerant hardware design and formal hardware verification using Verilog HDL
CO6	Design the digital circuits using CMOS transistor logic and the analog integrated circuits using Op-amps

Syllabus:

Introduction to RTL Design**:** Basic combinational (half adder, full adder, multiplexer, decoder, and so on) and sequential circuits design (Flip-flops and counters) using HDL with commercial VLSI CAD tools or open source compilers.

Familiarity of Datapath elements**:** 32-bit Ripple carry adder, recursive doubling based carry look ahead adder, Braun multiplier, Wallace tree multiplier, non-restoring based division, IEEE-754 floating point adder/Subtractor/multiplier/divider, CORDIC, modular multiplier, modular multiplicative inverse, modular exponentiator, cross-bar switch, Banyan switch, Batcher switch, digital FIR filter.

Advanced VLSI circuit design concepts**:** Pipelining, clock gating to reduce the switching power dissipation, hardware reuse strategy (folded hardware) to reduce the area, fault tolerant digital circuit design, formal hardware verification using equivalence check, high level synthesis with EDA, performance analysis of RTL design & high level synthesis based digital system using EDA, partial reconfiguration using EDA.

Hardware-Software Co-design**:** Design flow of hardware-software co-design using FPGA evaluation board with EDA, Custom IP design (arithmetic circuits as mentioned above), hardware-software partitioning, and performance analysis of various hardware-software co-design techniques.

Digital Circuits Design using CMOS**:** logic gates, combinational logic circuits, low power CMOS circuits using VLSI CAD tool.

Project Work (Individual): Basic 32-bit Processor Design (Harvard Architecture with Microprogramming based Controller) that includes the functional units such as logic unit, fixed/floating point adder, multiplier, and divider. Here, two separate memories are used for data and instruction.

Text Book(s):

1. Neil H.E. Westte and David Money Harris: CMOS VLSI Design : A Circuits and Systems Perspective, Addison Wesley, 4th Edn, 2011.

References & Web Resources:

1. Wakerly, J. F., Digital Design: Principles and Practices, 4th Edition, Pearson, 2008
2. Miron Abramovici, Melvin A Breuer, and Arthur D Friedman: Digital Systems Testing and Testable Designs, Wiley-IEEE Press, 1994.
3. N. A. Sherwani, Algorithms for VLSI Physical Design Automation, Bsp Books Pvt. Ltd., 3rd edition, 2005.
4. Samir Palnitkar: Verilog HDL - Guide to Digital design and synthesis, Pearson Education, 3rd Edn, 2003.

Semester-II Courses

Course Title	Course Code	Structure (I-P-C)		
Circuits for Electronic System Design	**EC504T**	**3**	**0**	**3**

Pre-requisite, if any: Analog and Digital Electronics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Apply concepts of Analog circuits for signal conditioning, signal processing, controller circuits, and driver circuits for power electronic circuits.
CO2	Design transformer and different power sources for various applications
CO3	Understand the interface of various modules to microcontroller and learn various communication protocols
CO4	Perform descriptive error analysis for the circuits
CO5	Demonstrate key concepts in electronics circuit design, including tools, approaches, and application scenarios

Syllabus:

Introduction to Op-Amps: Op-amp Characteristics, Negative feedback, Gain of the Op-Amp

Analog Signal conditioning circuits**:** Buffering, scaling, level translation, filtering applications, Analog math circuits - arithmetic circuits, log circuits, trigonometric circuits and applications Timer circuits, pulse width modulation circuits, P, PI and PID controller circuits, protection circuits, base and gate drive circuits for power transistors, MOSFETs and IGBTs, relay and contactor drive circuits. Design and error budget analysis of signal conditioners for low level AC and DC applications. Error Analysis.

Power supply circuits: Board level power supply circuits to generate +/-12V, 5V, 3.3V, 1.8V. Linear regulators, low drop out regulators, charge pumps, switched mode power converters.

Interfacing circuits**:** A to D, D to A, A to A and D to D interfaces, serial and parallel DACs, sampling, RS-232, USB, I2C, LCD, serial memory, SPI, CAN, wireless (RF, WiFi) Ethernet, RFID, SD card, SIM card, GPS, Touchscreen interfaces.

Digital circuit essentials**:** Digital filters, moving average, numeric formats, scaling, normalizing, arithmetic, log, exponential, square root, cube root, hypotenuse, sine, 3 phase waves, PWM etc.

References & Web Resources:

1. Franco, S., Design with operational amplifiers and analog integrated circuits. Mc. Graw Hill book Co. 1988.
2. Horowitz, P., and Hill, W., The art of electronics (2nd edition), Cambridge University Press. 1992.
3. Abraham Pressman, Keith Billings, Taylor Morey, Switching Power Supply Design, McGraw-Hill Education, 2009
4. Warwick A. Smith, ARM Microcontroller Interfacing: Hardware and Software, Elektor Electronics Publishing, 2010.

5. Datasheets and Application notes of different Integrated circuits.

Course Title	Course Code	Structure (I-P-C)		
Electronic Systems Packaging	**EC505T**	**3**	**0**	**3**

Pre-requisite, if any: Basics of Electrical & Electronics Engineering.

Course Aim: The course will sensitize the participants to the fundamentals of electronics systems packaging. The course is multidisciplinary in nature. Today products in the electronics industry need to be packaged to current state-of-art if it has to be in the leading edge market.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understands the electronics packaging including package styles or forms, hierarchy and methods of packaging necessary for various environments.
CO2	Provides industry perspective in the electronics packaging
CO3	Ability to distinguish between engineering performance and economic considerations to develop cost-efficient and high performance packaging approaches.
CO4	Predict the reliability of electronic components and structures.

Syllabus:

Overview Of Electronic Systems Packaging: Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products, Definition of PWB, Basics of Semiconductor and Process flowchart, Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire bonding, TAB and flip chip.

Electronic systems and needs, physical integration of circuits, packages, boards and complete electronic systems; system applications like computer, automobile, medical and consumer electronics with case studies and packaging levels.
:
Electrical design considerations - power distribution, signal integrity, RF package design and Power-delivery in systems. CAD for Printed Wiring Boards (PWBs) and Design for Manufacturability (DFM). PWB Technologies, Single-chip (SCM) and Multi-chip modules (MCM), flex circuits. Recent trends in manufacturing like microvias, sequential build-up circuits and high-density interconnect structures.

Materials and processes in electronics packaging, joining methods in electronics; lead-free solders. Surface Mount Technology – design, fabrication and assembly, embedded passive components.

Thermal management of IC and PWBs, Cooling Requirements, Electronic cooling methods thermo-mechanical reliability, design for reliability, electrical test and green packaging issues, Design for Reliability – Fundamentals, Induced failures. Electrical Testing – System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability. Trends in packaging.

References & Web Resources:

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001,
2. Rao R Tummala & Madhavan Swaminathan, Introduction to System-on-Package, McGraw Hill, 2008,
3. R S Khandpur, Printed Circuit Boards, McGraw Hill, 2006
4. Richard K. Ulrich &William D. Brown Advanced Electronic Packaging - 2nd Edition: IEEE Press, 2006.

Course Title	Course Code	Structure (I-P-C)		
Digital Signal Processing and Architectures	**EC506T**	**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems.

Course Aim: The goal of this course is to provide a good understanding of the principles and their corresponding hardware designs of various Digital Signal Processing operations.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concepts of digital signal processing: Filtering Techniques and Orthogonal Transformations.
CO2	Understand the working of DSP processors their architectures.
CO3	Develop the hardware designs of various digital Filtering Techniques and Orthogonal Transformations.

Syllabus:

Arithmetic Circuits – Fixed point number representation, barrel shifter, logarithmic shifter, ripple carry adder, carry select adder, carry skip adder, carry save adder, recursive doubling based carry look ahead adder, Booth algorithm, Carry save array multiplier, Wallace tree multiplier, distributed arithmetic based multiplication, fixed point multiply accumulate circuit design, restoring/non restoring division techniques, IEEE-754 floating point representation, floating point addition/subtraction, floating point multiplication/division, floating point multiply accumulate circuit design, and CORDIC.

Digital filter design-Basics of folded/parallel design, FIR/IIR filter design, steepest-descent LMS algorithm,

Adaptive FIR filter design, multirate signal processing, polyphase decomposition, and filter banks.

Discrete wavelet transform-Haar wavelet, 1D/2D-Convolution based discrete wavelet transform architecture, 1D/2D- (5,3) and (9,7) lifting based discrete wavelet transform architecture.

FFT architectures – radix-2/4 SDF, MDC, parallel FFT architectures.

HEVC architectures – discrete Hadamard transform architectures and integer DCT architectures.

Hardware/software co-design analogous between ASIC/FPGA/hardware-software co-designs, need for digital signal processing accelerators (or coprocessors), and hardware/software partitioning based digital signal processing architectures.

Digital signal processor design-basics of Von-Neumann, Harvard, Modified Harvard, and super Harvard architectures, hazards, hazard resolution techniques, instruction/data level parallelism

References & Web Resources:

1. Rafael C. Gonzalez and Richard E. Woods, Digital Image Processing, Pearson Education, 3rd Edition, 2009.
2. William K Pratt, Digital Image Processing, John Willey, 4th edition, 2006.
3. A.K. Jain, Fundamentals of Digital Image Processing, Prentice Hall of India, 1995.
4. Rafael C. Gonzalez, Richard E. Woods and Steven L. Eddins, Digital Image Processing using MATLAB, Pearson Education, 2nd Edition, 2009.
5. B. Chanda, D. Dutta Majumder, Digital Image Processing and Analysis, Prentice Hall of India, 2008.

Course Title	Course Code	Structure (I-P-C)		
Circuits for Electronic System Design Practice	**EC504P**	**0**	**3**	**2**

Pre-requisite, if any: Analog and Digital Electronics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and build circuits using OP-AMPS
CO2	Design and develop different power supplies
CO3	Design and develop signal conditioning circuits for resistive, capacitive, inductive, current and voltage-based sensors
CO4	Analysis of various communication protocols

Syllabus:

1. Design and build circuits using OPAMPS (summer, integrator, differentiators, and Instrumentation amplifier)
2. Design and build the power supply circuits such as linear power supply, LDO, and DC-DC converter
3. Design and develop the signal conditioning circuits for resistive (RTD), capacitive, inductive (LVDT), current (Photodiode) and voltage based sensors (Thermocouple)
4. Analysis of communication protocols (SPI, CAN, I2C)

References & Web Resources:

1. Franco, S., Design with operational amplifiers and analog integrated circuits. Mc. Graw Hill book Co. 1988.
2. Horowitz, P., and Hill, W., The art of electronics (2nd edition), Cambridge University Press. 1992.

3. Abraham Pressman, Keith Billings, Taylor Morey, Switching Power Supply Design, McGraw-Hill Education, 2009
4. Warwick A. Smith, ARM Microcontroller Interfacing: Hardware and Software, Elektor Electronics Publishing, 2010

Course Title	Course Code	Structure (I-P-C)		
Electronic Systems Packaging Practice	**EC505P**	**0**	**3**	**2**

Pre-requisite, if any: Basics of Electrical & Electronics Engineering.

Course Aim: To understand the manufacturing and assembling aspects of Electronic components in systems.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Expected to design optimized layout for printed circuits boards..
CO2	Exposed to multi-layer PCB design
CO3	To develop Prototype circuits

Syllabus:

PCB design flow- Schematic -layout - PCB design using created library -PCB printing using PCB prototyping machine-Testing and debugging of PCB

Familiarization of different components and chip packages

PCB Design for manufacturability

PCB Design consideration for special circuits

Design and development of PCBs using different simulator tools and prototyping.

Hands-on lab sessions for board manufacturing and assembly.

Thermal and Heat Sink Design

Electrical Testing and Active Circuit Testing

References & Web Resources:

1. Jan Axelson, Making Printed Circuit Boards, TAB/McGraw Hill, 1993
2. J. Varteresian, Fabricating Printed Circuit Boards.
3. Ronald A. Reis, Electronic project design and fabrication, 6/E, Prentice Hall, 2005.
4. Complete PCB Design Using OrCad Capture and Layout Kraig Mitzner, Elsevier.

Course Title	Course Code	Structure (I-P-C)		
Digital Signal Processing and Architectures Practice	**EC506P**	**0**	**3**	**2**

Pre-requisite, if any: Basic understanding of diode, transistor operation

Course Aim: The goal of this course is to provide a good understanding of the principles and their corresponding hardware designs of various Digital Signal Processing operations.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concepts of digital signal processing: Filtering Techniques and Orthogonal Transformations.
CO2	Develop the hardware designs of various digital Filtering Techniques and Orthogonal Transformations.

Syllabus:

Design of Datapath Blocks using in DSP: Adder, Multiplier, Divider, Multiply accumulate circuit, CORDIC, and so on.

Hardware/software co-design of signal processing operations

Digital Signal Co-processor design

Digital signal processor design-basics of Von-Neumann, Harvard, Modified Harvard, and super Harvard architectures

Digital Filter Designs – FIR, IIR, Adaptive filters

Discrete Orthogonal Transform Designs – FFT, integer DCT, DHT, DWT

References & Web Resources:

1. S. K. Mitra, Digital Signal Processing: A computer base approach, Third edition, McGraw Hill Higher Education, 2006.
2. Y.T. Chan, Wavelet Basics, Kluwer Publishers, Boston, 1993.
3. Simon Haykin, Adaptive filter theory, Pearson Education, Fifth edition, 2014.
4. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, and Naraig Manjikian, Computer Organization and Embedded Systems, McGraw Hill Publications, Sixth Edition, 2012.
5. A. V. Oppenheium, R. W. Schafer, Discrete-time signal processing, Second edition, Prentice Hall, 1999.
6. Moris M. Mano, Computer System Architecture, Third Edition, Pearson Publication, 2007.
7. John L. Hannessey and David A. Patterson, Computer Architecture: A Quantitative Approach, Fourth Edition, Elsevier, Morgan Kaufmann Publishers, 2007.

LIST OF ELECTIVES

Course Title	Course Code	Structure (I-P-C)		
Antenna Design	**EC511**	**3**	**0**	**3**

Pre-requisite, if any: Engineering Electromagnetics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Analyse a given Antenna
CO2	Measure a given Antenna
CO3	Design standard antennas
CO4	Develop new antenna structures with desired specifications

Syllabus:

Fundamental Concepts: Physical concept of radiation, Radiation pattern, near-and far-field regions, reciprocity, directivity and gain, effective aperture, polarization, input impedance, efficiency, Friis transmission equation, radiation integrals and auxiliary potential functions.

Radiation from Wires and Loops: Infinitesimal dipole, finite-length dipole, linear elements near conductors, dipoles for mobile communication, small circular loop.

Aperture and Reflector Antennas: Huygens' principle, radiation from rectangular and circular apertures, design considerations, Babinet's principle, Radiation from sectoral and pyramidal horns, design concepts, parabolic reflector and cassegrain antennas.

Broadband Antennas: Log-periodic and Yagi antennas, frequency independent antennas, Helical and Biconical antenna broadcast antennas, Spiral antenna.

Microstrip Antennas: Radiation mechanism, parameters and applications of microstrip antennas, feeding methods, methods of analysis, design of rectangular and circular patch antennas. Impedance matching of microstrip antenna.

Antenna systems and measurements: Receiving properties of antenna, Antenna noise and temperature, Gain measurement, polarization measurement, field intensity measurement, Antenna range Introduction and concept of antenna arrays. Case study on practical microstrip patch antenna for personal wireless communications consistent with the frequencies assigned by FCC.

Text Book(s):

1. C. A. Balanis, "Antenna Theory and Design", 3rd Ed., John Wiley & Sons., 2005.

2. W. L. Stutzman, and G. A. Thiele, "Antenna Theory and Design", 2nd Ed., John Wiley & Sons., 1998.

References & Web Resources:

1. R. E. Collin, "Antennas and Radio Wave Propagation", McGraw-Hill., 1985.
2. F. B. Gross, "Smart Antennas for Wireless Communications", McGraw-Hill., 2005
3. R. S. Elliot, "Antenna Theory and Design", Revised edition, Wiley-IEEE Press., 2003
4. J. D. Kraus and R. J. Marhefka, "Antennas for All Applications," Third Edition, 2002.
5. S. R. Saunders, "Antennas and Propagation for Wireless Communication Systems," John Wiley & Sons, 1999.

Course Title	Course Code	Structure (I-P-C)		
Analog and Mixed Signal Circuit Design	**EC512**	**3**	**0**	**3**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze complex analog integrated circuits using industry level analog IC Design tools
CO2	Design and analyze ADC and DAC using EDA tools
CO3	Design and analyze various MOSFET based arithmetic circuits.
CO4	Learn the various method of power optimization in analog circuits.

Syllabus:

Introduction: Review of single state MOS amplifiers, current mirrors, cascode current mirrors, active current mirrors, biasing techniques.

Op-amp design: Differential pair with current mirror load, single stage op-amp characteristics, single stage op-amo tradeoffs, telescopic cascode op-amp, folded cascode op-amp, two stage op-amp, fully differential single stage op-amp.

Data converter fundamentals: Analog versus digital (or discrete time) signals, converting analog signals to data signals, sample and hold circuits, sample and hold characteristics, switched capacitor circuits, DAC specifications, ADC specifications.

Data converters: DAC architectures – digital input code, R-2R ladder networks, current steering, charge scaling DACs, cyclic DAC, pipeline DAC, ADC architectures – flash ADC, 2-step flash ADC, pipeline ADC, integrating ADC, successive approximation ADC.

Phase locked loop: simple PLL, frequency/phase detectors, charge pump PLL, application as frequency multiplier.

Text Book(s):

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill International Edition 2016.

2. Baker, R. Jacob, CMOS: Circuit design, Layout, and Simulation. John Wiley & Sons, 2019.

References & Web Resources:

1. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2003.
2. Behzad Razavi, Fundamentals of Microelectronics, Second edition, Wiley, 2013
3. P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis And Design Of Analog Integrated Circuits, 5th edition, John Wiley & Sons, Inc., 2009.

Course Title	Course Code	Structure (I-P-C)		
Testing and Testability	**EC513**	**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Syllabus:

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models.

Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods.

Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Fault Diagnosis Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

Text Book(s):

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990
2. Stroud, "A Designer's Guide to Built-in Self-Test", Kluwer Academic Publishers, 2002

References & Web Resources:

1. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000
2. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
4. M. L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
5. P. K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
6. A. L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International.

Course Title	Course Code	Structure (I-P-C)		
Reliable Digital Communication System Design	**EC514**	**3**	**0**	**3**

Pre-requisite, if any: Communication Systems, Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Learn the functional behaviour of various cryptography, intrusion detection, and error correction algorithms.
CO2	Learn to develop hardware architectures of various cryptography, intrusion detection, and error correction algorithms.
CO3	Develop the countermeasure prototypes of adversary attacks
CO4	Develop the crypto co-processors using FPGA.

Syllabus:

Goals of Relilable Digital Communication: first level of defense (integrity, confidentiality, authenticity, and availability) and second level of defense (resilience to attacks).

Galois Field Arithmetic: Introduction to Group, Ring, and Fields, Prime/Polynomial field representation, Irreducible polynomial, primitive polynomial, minimal polynomial, Galois field addition, LSB first/MSB first/Montgomery Galois field multiplication architectures-bit serial, bit parallel, digit serial, systolic, and scalable architectures, Modular exponentiators-Square-multiply algorithm and Montgomery Ladder algorithm, Extended Euclidean algorithm/Fermat's little theorem based multiplicative inverse architectures.

Symmetric Encryption/Decryption Architectures: DES, 3-DES, and AES (fully folded, parameterized parallel, and fully parallel architectures).

Asymmetric Encryption/Decryption Architectures: ECC (right-to-left, left-to-right, Montgomery based scalar multiplication in affine/projective co-ordinates) and RSA.

HASH architectures: SHA512 and SHA3.

Key exchange protocols: Diffie Helmen, Elgamal, Neuro crypto key exchange protocol.

Authentication schemes: Yang Shieh and Eiji Okamato.

Pseudo random number generators, Stream ciphers.

Physical unclonable functions: RO PUF, larger decoder memory based PUF, and XOR PUF.

Intrusion Detection: Universal HASH functions, Cuckoo hashing, and Bloom filter.
Error detection codes: CRC, LRC, and parity check, Error correction codes-Hamming, BCH, Reed Solomon, LDPC, Convolutional, Turbo product, and concatenated codes,
Hardware/software co-design analogous between ASIC/FPGA/hardware-software co-designs, need for crypto accelerators (or coprocessors), and hardware/software partitioning based AES/ECC architectures.

Side channel analysis: Power attack, Bit masking, and Cache template attack.

Text Book(s):

1. Doug R. Stinson , Cryptography Theory and Practice, Third Edition, CRC Press, 2006.
2. Shu Lin and Daniel J Castello, Error Control Coding, Second Edition, Printice Hall, 2004.

References & Web Resources:

1. A. J. Menezes, P. C. van Oorshot, and S. A. Vanstone, Handbook of Applied Cryptography, CRC Press, 1996.
2. Jonathan Katz and Yehuda Lindell, Introduction to Modern Cryptography, CRC Press, 2015.
3. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, Hardware Security: Design, Threats and Safeguards, CRC Press, 2014.

Course Title	Course Code	Structure (I-P-C)		
Satellite Communication	**EC515**	**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the satellite communication.
CO2	Understand the orbits and space of satellite communication.
CO3	Understand the optical communication.
CO4	Develop the packet switched networks.

Syllabus:

OVERVIEW OF SATELLITE SYSTEMS, ORBITS AND LAUNCHING METHODS: Introduction, Frequency Allocations for Satellite Services, Intelsat, U. S. Domsats Polar Orbiting Satellites, Problems, Kepler's First Law, Kepler's Second Law, Kepler's Third Law, Definitions of Terms for Earth-orbiting Satellites, Orbital Elements, Apogee and Perigee Heights, Orbital Perturbations, Effects of a Non-spherical Earth, Atmospheric Drag, Inclined Orbits, Calendars, Universal Time, Julian Dates, Sidereal Time, The Orbital Plane, The Geocentric, Equatorial Coordinate System, Earth Station Referred to the IJK Frame, The Top centric-Horizon Co-ordinate System, The Sub-satellite Point, Predicting Satellite Position.

GEOSTATIONARY ORBIT & SPACE SEGMENT: Introduction, Antenna Look Angels, The Polar Mount Antenna , Limits of Visibility , Near Geostationary Orbits, Earth Eclipse of Satellite, Sun Transit Outage, Launching Orbits, Problems, Power Supply, Attitude Control, Spinning Satellite Stabilization, Momentum Wheel Stabilization, Station Keeping, Thermal Control, TT&C Subsystem , Transponders, Wideband Receiver, Input De-multiplexer, Power Amplifier, Antenna Subsystem, Morelos, Anik-E, Advanced Tiros-N Spacecraft.

OPTICAL NETWORK ARCHITECTURES: Introduction to Optical Networks; Layered Architecture- Spectrum partitioning, Network Nodes, Network Access Stations, Overlay Processor, Logical network overlays, Connection Management and Control; Static and Wavelength Routed Networks; Linear Light wave networks; Logically Routed Networks; Traffic Grooming; The Optical Control Plane- Architecture, Interfaces, Functions; Generalized Multiprotocol Label Switching – MPLS network and protocol stack, Link management, Routing and Signaling in GMPLS.

OPTICAL PACKET SWITCHED NETWORKS: Network Architectures- Unbuffered Networks, Buffering Strategies; OPS enabling technologies, Test beds; Optical Burst Switching, Switching protocols, Contention Resolution, Optical Label Switching, OLS network test beds, Control and Management – Network management functions, Configuration management, Performance management, Fault management, Optical safety, Service interface; network Survivability- Protection in SONET / SDH and IP Networks, Optical layer Protection, Interworking between layers.

FREE SPACE OPTICAL COMMUNICATION: Analog and digital FSOC data link, atmospheric attenuation, scattering, scintillation index, beam wandering, beam wave front aberration, adaptive optics, active optics, deformable mirror control, RoFSO, atmospheric

channel models, estimation of refractive index, modulation and demodulation techniques, error control techniques.

Text Book(s):

1. Satellite Communications, Dennis Roddy, McGraw-Hill Publication Third edition2001
2. Satellite Communications – Timothy Pratt, Charles Bostian and Jeremy Allnutt, WSE, Wiley Publications, 2nd Edition, 2003.

References & Web Resources:

1. Timothy Pratt – Charles Bostian & Jeremy Allmuti, Satellite Communications, John Willy & Sons (Asia) Pvt. Ltd. 2004
2. Wilbur L. Pritchars Henri G. Suyder Hond Robert A. Nelson, Satellite Communication Systems Engineering, Pearson Education Ltd., Second edition 2003.
3. Satellite Communications: Design Principles – M. Richharia, BS Publications, 2nd Edition, 2003.
4. J. Gower, "Optical Communication System", Prentice Hall of India, 2001
5. Rajiv Ramaswami, "Optical Networks ", Second Edition, Elsevier, 2004.
6. Satellite Communications Engineering – Wilbur L. Pritchard, Robert A Nelson and Henri G. Suyderhoud, 2nd Edition, Pearson Publications, 2003.
7. Optical Fiber Communication – John M. Senior – Pearson Education – Second Edition. 2007
8. Optical Fiber Communication – Gerd Keiser – Mc Graw Hill – Third Edition. 2000

Course Title	Course Code	Structure (I-P-C)		
Design of IoT System	**EC516**	**3**	**0**	**3**

Pre-requisite, if any: Microprocessors and Microcontrollers.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the networking with IoT, its enabling technologies, and explore a young, but rich, body of exciting ideas, solutions, and paradigm shifts.
CO2	Understanding the potential of IoT devices, support for networking according to the protocol standards, and being able to program them, would be useful for real time applications.
CO3	Develop the rapid prototypes of IoT based embedded systems using sensors, cloud.
CO4	Develop the IoT system using Arduino, Raspberry Pi, BeagleBone Black, and Intel Edison/Galileo.

Syllabus:

Introduction to IoT: Definition, Trend, IoT applications, Sensing and Actuation, IoT Devices and deployment models, Power awareness of IoT, LDO in IoT.

IoT Networking: Basic IoT Components, Interdependencies, Service Oriented Architecture.

IoT Data Protocols: MQTT, SMQTT, CoAP, XMPP, AMQP.

IoT Communication Protocols and their applications: IEEE 802.15.4, ZigBee6LoWPAN, Wireless HART, Z-Wave, ISA 100, Bluetooth, and Bluetooth low energy (BLE), NFC, RFID, WiFi for IoT communications.

Data Handling, Analytics, Data management for IoT: Data cleaning and processing, Data storage models, Searching in IoT, Deep Web Semantic Sensor Web, Semantic web data management, Real-time and Big data analytics for IoT, High-dimensional data processing, Parallel and Distributed data processing.

Interoperability in IoT: Low power Interoperability for IPV6 IoT.

Cloud-Centric IoT: Architecture, Open Challenges, Energy efficiency, QoS, QoE.

Industrial IoT (IIoT): Industrial IoT and its benefits, Future of IIoT, Challenges, Examples.

IoT System Management and Virtualization: IoT environment management over Cloud computing framework, Fog Computing paradigm for IoT with case studies, Softwarized control and virtualization technologies for IoT network and computation resource managements.

Case Studies: Sensor body-area-network, Smart cities and Smart homes, Agriculture.

IoT Network Framework: Wireless Network Fundamental for IoT communication tutorials with demonstrations and hands-on: 802.11 and 802.15.4 MAC Fundamentals, Management Operations, Security Overview, Network Core Protocols, Tizen Network Stack Architecture, Introduction, CAPI Architecture Overview, Sync/Async Operation Sequence, Interaction of Network Core Components, P2P Core Component Overview, OEM Layer, Supplicant Plugin Architecture overview.

Text Book(s):

1. The Internet of Things: Enabling Technologies, Platforms, and Use Cases, by EethurumRaj and Anupama C. Raman (CRC Press).
2. Internet of Things: A Hands-on Approach, by Arshdeep Bahga and Vijay Madisetti (Universities Press).

References & Web Resources:

1. Adrian McEwen, Hakim Cassimally, Designing the Internet of Things, Wiley,Nov 2013, (1st edition)
2. Martin Charlier, Alfred Lui, Claire Rowland, Elizabeth Goodman, Ann Light, Designing Connected Products, May 2015, O'Reilly Media.

Course Title	Course Code	Structure (I-P-C)		
Data Communication and Networking	**EC517**	**3**	**0**	**3**

Pre-requisite, if any: Computer Networks, C Programming

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand a transmission of a data in a network
CO2	Acquire knowledge of various OSI layers.
CO3	Understand topologies for specific networks.
CO4	Understand the basics of cryptography.

Syllabus:

Overview of Data Communication and Networking: Introduction; Data communications: components, data representation (ASCII, ISO etc.), direction of data flow (simplex, half duplex, full duplex); network criteria, physical structure (type of connection, topology), categories of network (LAN, MAN, WAN); Internet: brief history, Protocols and standards; Reference models: OSI reference model, TCP/IP reference model, their comparative study.

Physical Layer: Overview of data (analog & digital), signal (analog & digital), transmission (analog & digital) & transmission media (guided & unguided); Circuit switching: time division & space division switch, TDM bus; Telephone Network; ATM, B-ISDN.

Data link Layer: Types of errors, framing (character and bit stuffing), error detection & correction methods; Flow control; Protocols: Stop & wait ARQ, Go-Back- N ARQ, Selective repeat ARQ, HDLC.

Medium Access sublayer: Point to Point Protocol, LCP, NCP, Token Ring; Reservation, Polling, Multiple access protocols: Pure ALOHA, Slotted ALOHA, CSMA, CSMA/CD, CSMA/CA Traditional Ethernet, fast Ethernet (in brief).

Network layer: Internetworking & devices: Repeaters, Hubs, Bridges, Switches, Router, Gateway; Addressing: IP addressing, subnetting; Routing: techniques, static vs. dynamic routing, Unicast Routing Protocols: RIP, OSPF, BGP; Other Protocols: ARP, IP, ICMP, IPV6.

Transport layer: Process to Process delivery; UDP; TCP; Congestion Control: Open Loop, Closed Loop choke packets; Quality of service: techniques to improve QoS: Leaky bucket algorithm, Token bucket algorithm.

Application Layer: Introduction to DNS, SMTP, SNMP, FTP, HTTP & WWW; Security: Cryptography (Public, Private Key based), Digital Signature, Firewalls.

Text Book(s):

1. B. A. Forouzan, Data Communications and Networking, 4th edition, Tata McGraw Hill 2012, ISBN: 0072967757
2. A. S. Tanenbaum, Computer Networks, 4th edition, Pearson, 2013, ISBN: 978-0132126953

References & Web Resources:

1. W. Stallings, Data and Computer Communications, 5th edition, Pearson, 5th edition, 2013, ISBN: 978-0133506488.

Course Title	Course Code	Structure (I-P-C)		
Numerical Techniques in Electromagnetics	**EC521**	**3**	**0**	**3**

Pre-requisite, if any: Engineering Electromagnetics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand various computational techniques and their pros and cons.
CO2	Understand which software works best in terms of speed, and accuracy for analysing a given structure
CO3	Develop codes to analyze the EM structures.
CO4	Develop EM simulation software tools

Syllabus:

Review of vector calculus, Overview of computational electromagnetics, Review of Maxwell's equations.
Analytical techniques in Electromagnetics.
Finite Difference Time Domain methods: Analysis, convergence, accuracy and numerical dispersion,incorporating dielectric and dispersive materials, absorbing boundary conditions, perfectly matched layers (PML), sources.

Moment Methods: Integral equations (EFIE,MFIE), Green's Functions, MOM.

Finite element methods: Formulation and Absorbing boundary conditions (FEM).

Applications of computational electromagnetics: Specific Absorption Rate, Radar RCS, Periodic structures, Eddy current calculations, capacitance and inductance calculations, Microwave inverse imaging, Antenna radiation problems, Calculating the modes of a waveguide structure using the integral equation method.

Text Book(s):

1. Numerical Techniques in Electromagnetics, Second Edition Hardcover – Import, 12 July 2000, by Matthew N.O. Sadiku
2. Analytical and Computational Methods in Electromagnetics, Artech House Electromagnetic Analysis, 30 September 2008, by Ramesh Garg, Raj Mittra

References & Web Resources:

1. Computational Electromagnetics for RF and Microwave Engineering, 28 October 2010, by David B. Davidson
2. Advanced Engineering Electromagnetics Paperback - 8 October 2008, by Constantine A. Balanis
3. Computational Methods for Electromagnetics: 4 (IEEE Press Series on Electromagnetic Wave Theory) Hardcover – Import, 12 December 1997, by Andrew F. Peterson, Scott L. Ray, Raj Mittra

Course Title	Course Code	Structure (I-P-C)		
RF and Microwave Integrated Circuits	**EC522**	**3**	**0**	**3**

Pre-requisite, if any: Engineering Electromagnetics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Analyse high frequency filters, couplers, amplifier, oscillators and mixer circuits.
CO2	Design high frequency filters, couplers, amplifiers.
CO3	Develop RFICs.
CO4	Develop MMICs.

Syllabus:

Electromagnetic Theory Review: Maxwell's Equations, Fields in Media and Boundary Conditions, The Wave Equation, General Plane Wave Solutions, Energy and Power, Transmission lines and waveguide solutions.

Transmission Line Theory: The Lumped-Element Circuit Model for a Transmission Line, Field Analysis of Transmission Lines, The Terminated Lossless Transmission Line, The Smith Chart, The Quarter-Wave Transformer, Generator and Load Mismatches, Lossy Transmission Lines, Transients on Transmission Lines.

Microwave Network Analysis: Impedance and Equivalent Voltages and Currents, Impedance and Admittance Matrices, The Scattering Matrix, The Transmission (ABCD) Matrix.

Impedance matching and tuning, Microwave filter design.

Noise and nonlinear distortion, active rf and microwave devices.

Microwave Power Amplifier, Low Noise Amplifier, Oscillator and Mixer Design.

Introduction to microwave systems.

Text Book(s):

1. David M Pozar, Microwave Engineering, 4th Edition, Wiley, 2013.

References & Web Resources:

1. Robert E Collin, Foundations for Microwave Engineering, 2nd Edition, Wiley, 2007.
2. Behzad Razavi, RF Microelectronics, 2nd Edition, Pearson, 2011.
3. I.D. Robertson, S. Lucyszyn, RFIC and MMIC Design and Technology: 13 (Materials, Circuits and Devices), Institution of Engineering and Technology, 2001.

Course Title	Course Code	Structure (I-P-C)		
Electromagnetic Interference and Compatibility	**EC523**	**3**	**0**	**3**

Pre-requisite, if any: Engineering Electromagnetics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Gain knowledge to understand the concept of EMI / EMC related to product design.
CO2	Diagnose and solve various electromagnetic compatibility problems.
CO3	Understand the sources of EMI and various coupling methods.
CO4	Learn the various method of doing the pre compliance measurement techniques.

Syllabus:

Introduction to EMI and EMC: Various EMC requirements and standards-Need for EMC and its importance in electronic product design - sources of EMI - few case studies on EMC.

Conducted and radiated emission: power supply line filters-common mode and differential mode current-common mode choke- switched mode power supplies.

Shielding techniques: shielding effectiveness-shield behavior for electric and magnetic field - aperture-seams-conductive gaskets- conductive coatings.

Grounding techniques: signal ground-single point and multi point grounding-system ground common impedance coupling -common mode choke-Digital circuit power distribution and grounding.

Contact protection: arc and glow discharge-contact protection network for inductive loads-C, RC, RCD protection circuit- inductive kick back.

RF and transient immunity: transient protection network- RFI mitigation filter-power line disturbance- ESD- human body model- ESD protection in system design.

PCB design for EMC compliance: PCB layout and stack up- multi layer PCB objectives Return path discontinuities-mixed signal PCB layout.

EMC pre compliance measurement: conducted and radiated emission test-LISN- Anechoic chamber.

Text Book(s):

1. H. W. Ott, Electromagnetic Compatibility Engineering, 2nd edition, John Wiley & Sons, 2011, ISBN: 9781118210659.

2. C. R. Paul, Introduction to Electromagnetic Compatibility, 2nd edition, Wiley India, 2010, ISBN: 9788126528752.

References & Web Resources:

1. K. L. Kaiser, Electromagnetic Compatibility Handbook, 1st edition, CRC Press, 2005. ISBN: 9780849320873.

Course Title	Course Code	Structure (I-P-C)		
Software Defined Radio	**EC524**	**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the SDR, CR, and their applications.
CO2	Understand the signal processing architectures used in the SDR.
CO3	Develop the FPGA based SDR.
CO4	Develop microcontroller based SDR.

Syllabus:

INTRODUCTION TO SDR: What is Software-Defined Radio, The Requirement for Software-Defined Radio, Legacy Systems, The Benefits of Multi-standard Terminals, Economies of Scale, Global Roaming, Service Upgrading, Adaptive Modulation and Coding, Operational Requirements, Key Requirements, Reconfiguration Mechanisms, , Handset Model, New Base-Station and Network, Architectures, Separation of Digital and RF, Tower-Top Mounting, BTS Hoteling, Smart Antenna Systems, Smart Antenna System Architectures, Power Consumption Issues, Calibration Issues, Projects and Sources of Information on Software Defined Radio.

BASIC ARCHITECTURE OF A SOFTWARE DEFINED RADIO: Software Defined Radio Architectures, Ideal Software Defined Radio Architecture, Required Hardware Specifications, Digital Aspects of a Software Defined Radio, Digital Hardware, Alternative Digital Processing Options for BTS Applications, Alternative Digital Processing Options for Handset Applications, Current Technology Limitations, A/D Signal-to-Noise Ratio and Power 343 Consumption, Derivation of Minimum Power Consumption, Power Consumption Examples, ADC Performance Trends, Impact of Superconducting Technologies on Future SDR Systems.

SIGNAL PROCESSING DEVICES AND ARCHITECTURES: General Purpose Processors, Digital Signal Processors, Field Programmable Gate Arrays, Specialized Processing Units, Tilera Tile Processor, Application-Specific Integrated Circuits, Hybrid Solutions, Choosing a DSP Solution. GPP-Based SDR, Non real time Radios, High-Throughput GPP-Based SDR, FPGA-Based SDR, Separate Configurations, Multi-Waveform Configuration, Partial

Reconfiguration, Host Interface, Memory-Mapped Interface to Hardware, Packet Interface, Architecture for FPGA-Based SDR, Configuration, Data Flow, Advanced Bus Architectures, Parallelizing for Higher Throughput, Hybrid and Multi-FPGA Architectures, Hardware Acceleration, Software Considerations, Multiple HA and Resource Sharing, Multi-Channel SDR.

COGNITIVE RADIO : TECHNIQUES AND SIGNAL PROCESSING History and background, Communication policy and Spectrum Management, Cognitive radio cycle, Cognitive radio architecture, SDR architecture for cognitive radio, Spectrum sensing Single node sensing: energy detection, cyclostationary and wavelet based sensing- problem formulation and performance analysis based on probability of detection vs SNR. Cooperative sensing: different fusion rules, wideband spectrum sensing- problem formulation and performance analysis based on probability of detection vs SNR.

COGNITIVE RADIO: HARDWARE AND APPLICATIONS: Spectrum allocation models. Spectrum handoff, Cognitive radio performance analysis. Hardware platforms for Cognitive radio (USRP, WARP), details of USRP board, Applications of Cognitive radio.

Text Book(s):

1. "RF and Baseband Techniques for Software Defined Radio" Peter B. Kenington, ARTECH HOUSE, INC © 2005.
2. "Implementing Software Defined Radio", Eugene Grayver, Springer, New York Heidelberg Dordrecht London, ISBN 978-1-4419-9332-8 (eBook) 2013.

References & Web Resources:

1. "Cognitive Radio Technology", by Bruce A. Fette, Elsevier, ISBN 10: 0-7506-7952-2, 2006.
2. "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", Hüseyin Arslan, Springer, ISBN 978-1-4020-5541-6 (HB), 2007.

Course Title	Course Code	Structure (I-P-C)		
Cognitive Communication Networks	**EC525**	**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the Cognitive Communication and networking as per applications.
CO2	Detect the desired signal in scrambled spectrum.
CO3	Understand algorithms for of cognitive networks.
CO4	Understand the MAC protocols in cognitive networks.

Syllabus:

Introduction to Cognitive Radio: Introduction –Software Defined Radio: Architecture–Digital Signal Processor and SDR Baseband architecture – Reconfigurable Wireless Communication Systems – Digital Radio Processing –Cognitive Radio: Cognitive radio Framework – Functions – Paradigms of Cognitive Radio.

Spectrum Sensing: Introduction –Spectrum Sensing – Multiband Spectrum Sensing – Sensing Techniques – Other algorithms – Comparison – Performance Measure & Design Trade-Offs: Receiver operating characteristics – Throughput Performance measure –Fundamental limits and trade-offs.

Cooperative Spectrum Acquisition: Basics of cooperative spectrum sensing–Examples of spectrum acquisition techniques – cooperative transmission techniques – sensing strategies– Acquisition in the Presence of Interference: Chase combining HARQ –Regenerative cooperative Diversity– spectrum overlay– spectrum handoff.

MAC Protocols and Network Layer Design: Functionality of MAC protocol in spectrum access –classification –Interframe spacing and MAC challenges – QOS – Spectrum sharing in CRAHN –CRAHN models – CSMA/CA based MAC protocols for CRAHN – Routing in CRN– Centralized and Distributed protocols – Geographical Protocol.

Text Book(s):

1. Mohamed Ibnkahla, "Cooperative Cognitive Radio Networks:The complete Spectrum Cycle" I edition.
2. AhamedKhattab, Dmitri Perkins,BagdyByoumi,"Cognitive Radio Networks from Theory to practice" 2013th edition.

References & Web Resources:

1. Kwang-Cheng Chen and Ramjee Prasad, "Cognitive Radio Networks, Wiley Pub
2. Alexander M.Wyglinski,MaziarNekovee, ThomasHou," Cognitive Radio Communications and Networks". I edition.

Course Title	Course Code	Structure (I-P-C)		
MIMO Communication Systems	**EC526**	**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concept of MIMO communication techniques, Channel Capacity, MIMO algorithms.
CO2	Understand power allocation strategies for practical MIMO systems.
CO3	Design algorithms of MIMO to improve the bit rate.
CO4	Understand MIMO in 5G communication.

Syllabus:

Introduction: Diversity-multiplexing trade-off, transmit diversity schemes, advantages and applications of MIMO systems.

Analytical MIMO channel models: Uncorrelated, fully correlated, separately correlated and keyhole MIMO fading models, parallel decomposition of MIMO channel.

Power allocation in MIMO systems:Uniform, adaptive and near optimal power allocation.

MIMO channel capacity: Capacity for deterministic and random MIMO channels, Capacity of i.i.d., separately correlated and keyhole Rayleigh fading MIMO channels.

Space-Time codes: Advantages, code design criteria, Alamouti space-time codes, SER analysis of Alamouti space-time code over fading channels, Space-time block codes, Space-time trellis codes, Performance analysis of Space-time codes over separately correlated MIMO channel, Space-time turbo codes.

MIMO detection: ML, ZF, MMSE, ZF-SIC, MMSE-SIC, LR based detection.

Advances in MIMO wireless communications: Spatial modulation, MIMO based cooperative communication and cognitive radio, multiuser MIMO, cognitive-femtocells and large MIMO systems for 5G wireless.

Text Book(s):

1. R. S. Kshetrimayum, Fundamentals of MIMO Wireless Communications, Cambridge University Press, 2017.
2. A. Chokhalingam and B. S. Rajan, Large MIMO systems, Cambridge University Press, 2014.

References & Web Resources:

1. B. Kumbhani and R. S. Kshetrimayum, MIMO Wireless Communications over Generalized Fading Channels, CRC Press, 2017
2. T. L. Marzetta, E. G. Larsson, H. Yang and H. Q. Ngo, Fundamentals of Massive MIMO, Cambridge University Press, 2016.

Course Title	Course Code	Structure (I-P-C)		
Detection and Estimation Theory	**EC527**	**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Random Process, Communication Systems

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the discrete-time and continuous-time signal theory for finding unknown signal parameters.
CO2	Extract useful information from random observations in communications.
CO3	Design and analyze optimum detection schemes.
CO4	Estimate the error in wireless communication.

Syllabus:

Detection Theory: Detection Theory in Signal Processing; the Detection Problem; the Mathematical Detection Problem; Hierarchy of Detection Problems; Role of Asymptotics.

Statistical Detection Theory: Neyman-Pearson Theorem , Receiver Operating Characteristics, Minimum Probability of Error, Multiple Hypothesis Testing, Minimum Bayes Risk Detector - Binary Hypothesis.

Deterministic Signal: Matched Filters – Development of Detector, Performance of Matched Filter; Multiple Signals – Binary case, Performance of Binary Case, M-ary case.
Random Signals: Estimator-Correlator – Energy Detector; Linear Model - Rayleigh Fading Sinusoid, Incoherent FSK for a Multipath Channel.

Estimation Theory: Estimation in Signal Processing; Mathematical Estimation Problem; Assessing Estimator Performance.

Minimum Variance Unbiased Estimation: Unbiased Estimators; Minimum Variance Criterion; Existence of the Minimum Variance Unbiased Estimator; Finding the Minimum Variance Unbiased Estimator. Estimator Accuracy Considerations; Cramer-Rao Lower Bound; General CRLB for Signals in AWGN.

Estimation Techniques: Linear Model, General Minimum Variance Unbiased Estimation, Best Linear Unbiased Estimators, Maximum Likelihood Estimation, Least Squares, Estimation.

Text Book(s):

1. Steven M. Kay, Fundamentals of Statistical signal processing, volume-1: Estimation theory. Prentice Hall 2011.
2. Steven M. Kay, Fundamentals of Statistical signal processing, volume-2: Detection theory. Prentice Hall 2011.

References & Web Resources:

1. Harry L. Van Trees, Detection, Estimation, and Modulation Theory, Part I, John Wiley & Sons, Inc. 2011.
2. A. Papoulis and S. Unnikrishna Pillai, Probability, Random Variables and stochastic processes, 4e. The McGraw-Hill 2010.

Course Title	Course Code	Structure (I-P-C)		
Electric Vehicle Technology	**EC528**	**3**	**0**	**3**

Pre-requisite, if any: Basic Electrical and Electronics Engineering, Electric Drives

Course Outcomes: At the end of the course, the students will be able to:

CO1	To understand about basics of electric vehicle

CO2	To understand drives and control.
CO3	Select battery, battery indication system for EV applications
CO4	Design battery charger for an EV

Syllabus:

Introduction to Electric Vehicle : Review of Conventional Vehicle: Introduction to Electric Vehicles: Types of EVs, Electric Drive-train, Tractive effort in normal driving.

Electric Drives : Basic concept of electric traction, introduction to various electric drive-train topologies, power flow control in electric drive-train topologies, fuel efficiency analysis. Introduction to electric components used in hybrid and electric vehicles, Configuration and control of DC Motor drives, Configuration and control of Induction Motor drives, configuration and control of Permanent Magnet Motor drives, Configuration and control of Switch Reluctance Motor drives, drive system efficiency.

Energy Storage : Introduction to Energy Storage Requirements in Electric Vehicles: - Battery based energy storage and its analysis, Fuel Cell based energy storage and its analysis, Hybridization of different energy storage devices. Sizing the drive system, Sizing the propulsion motor, sizing the power electronics, selecting the energy storage technology, Communications, supporting subsystems.

Energy Management System : Energy Management Strategies, Automotive networking and communication, EV charging standards, V2G, G2V, V2B, V2H. Business: E-mobility business, electrification challenges, Business- E-mobility business, electrification challenges.

Mobility and Connectors : Connected Mobility and Autonomous Mobility- case study E-mobility Indian Roadmap Perspective. Policy: EVs in infrastructure system, integration of EVs in smart grid, social dimensions of EVs. Connectors- Types of EV charging connector, North American EV Plug Standards, DC Fast Charge EV Plug Standards in North America, CCS (Combined Charging System), CHAdeMO, Tesla, European EV Plug Standards.

Text Book(s):

1. Emadi, A. (Ed.), Miller, J., Ehsani, M., “Vehicular Electric Power Systems” Boca Raton, CRC Press, 2003
2. Husain, I. “Electric and Hybrid Vehicles” Boca Raton, CRC Press, 2010.

References & Web Resources:

1. Larminie, James, and John Lowry, “Electric Vehicle Technology Explained” John Wiley and Sons, 2012
2. Tariq Muneer and Irene IllescasGarcía, “The automobile, In Electric Vehicles: Prospects and Challenges”, Elsevier, 2017
3. 5. Sheldon S. Williamson, “Energy Management Strategies for Electric and Plug-in Hybrid Electric Vehicles”, Springer, 2013
4. Patents of TESLA

Course Title	Course Code	Structure (I-P-C)		
Navigation System	**EC529**	**3**	**0**	**3**

Pre-requisite, if any: Nil

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concept of GNSS, AGNSS, Radio Positioning and Integration of Navigation technique.
CO2	Analyze navigation in various terrestrial situations.
CO3	Find the exact location of an object in the navigation system.
CO4	Design precision navigation systems.

Syllabus:

INTRODUCTION TO NAVIGATION: What Is Navigation, Position Fixing, Dead Reckoning, Inertial Navigation, Radio and Satellite Navigation, Terrestrial Radio Navigation, Satellite Navigation, Feature Matching, The Complete Navigation System.

NAVIGATION MATHEMATICS: Coordinate Frames, Kinematics, and the Earth: Coordinate Frames, Kinematics, Earth Surface and Gravity Models, Frame Transformations, Coriolis force.

INERTIAL NAVIGATION: Inertial-Frame Navigation Equations, Earth-Frame Navigation Equations, Local-Navigation-Frame Navigation Equations, Navigation Equations Precision, Initialization and Alignment, INS Error Propagation, Platform INS, Horizontal-Plane Inertial Navigation.

PRINCIPLES OF RADIO POSITIONING: Radio Positioning Configurations and Methods, Positioning Signals, User Equipment, Propagation, Error Sources, and Positioning Accuracy.

GNSS: FUNDAMENTALS, SIGNALS, AND SATELLITES: Fundamentals of Satellite Navigation, The Systems: Global Positioning System, GLONASS, Galileo, Beidou, REGIONAL NAVIGATION SYSTEMS: Beidou and Compass, QZSS, IRNSS, GNSS INTEROPERABILITY: Frequency Compatibility, User Competition, Multistandard User Equipment Augmentation Systems, System Compatibility, GNSS Signals, Navigation Data Messages.

ADVANCED SATELLITE NAVIGATION: Differential GNSS, Carrier-Phase Positioning and Attitude, Poor Signal-to-Noise Environments, Multipath Mitigation, Signal Monitoring, Semi-Codeless Tracking.

TERRESTRIAL RADIO NAVIGATION: Point-Source Systems, Loran, Instrument Landing System, Urban and Indoor Positioning, Relative Navigation, Tracking, Sonar Transponders. (

FEATURE MATCHING: Terrain-Referenced Navigation, Sequential Processing, Batch Processing, Performance, Laser TRN, Barometric TRN, Sonar TRN, Image Matching, Scene

Matching by Area Correlation, Continuous Visual Navigation, Map Matching, Other Feature-Matching Techniques, Stellar Navigation, Gravity Gradiometry, Magnetic Field Variation. (6 hours)
INS/GNSS Integration: Integration Architectures, System Model and State Selection, Measurement Models, Advanced INS/GNSS Integration.

Text Book(s):

1. Principles of GNSS, Inertial, and Multisensor Integrated Navigation Systems, Paul D. Groves Artech House, 2008 and 2013 Second Edition.
2. B.Hofmann Wollenhof, H.Lichtenegger, and J.Collins, "GPS Theory and Practice", Springer Wien, New York, 2000.

References & Web Resources:

1. Pratap Misra and Per Enge, "Global Positioning System Signals, Measurements, and Performance," Ganga-Jamuna Press, Massachusetts, 2001.
2. Ahmed El-Rabbany, "Introduction to GPS," Artech House, Boston, 2002.
3. Bradford W. Parkinson and James J. Spilker, "Global Positioning System: Theory and Applications," Volume II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.

भारतीय सूचना प्रौद्योगिकी अभिकल्पना एवं विनिर्माण संस्थान , कर्नूल
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
DESIGN AND MANUFACTURING KURNOOL
Jagannathagattu, Kurnool – 518007, Andhra Pradesh, INDIA
(An Institute of National Importance under the Ministry of Education, Govt. of India)

ORDINANCES and REGULATIONS

for

Master of Technology Programme

Effective from the A.Y. 2020-21

(July 2020)

ORDINANCE

O.1 The minimum academic qualification for admission through CCMT to IIITDM Kurnool is 60% or 6.5 CGPA in the appropriate branch of engineering or its equivalent.

a. Candidates who have qualified for the award of the Bachelor's degree in Engineering / Technology from educational Institutions approved by AICTE/UGC/Government and who have a valid GATE (Graduate Aptitude Test in Engineering) score are eligible to apply for admission to the M.Tech programme.

b. Associate Membership holders of the professional bodies for admission into their parent disciplines from the following – (i) The Institution of Engineers (India) (AMIE) (ii) The Indian Institute of Metals (AMIM) (iii) The Institution of Electronics and Tele- communication Engineering (AMIETE) with valid GATE Score can also apply.

O.2 Candidates working and sponsored (with full pay and allowances for 24 months) by industry / government organizations / private and public enterprises recognized by DST and engaged in R & D work/ engineering colleges recognized by AICTE / UGC, possessing at least two years of professional experience as on the last date of receipt of applications at IIITDM, Kurnool, can apply, provided they hold:

1. B.E./ B.Tech. degree from AICTE/UGC recognized Engineering Colleges/university with first class or 60% aggregate marks in all the four years or

2. AMIE and other Associate memberships (listed above) with a valid GATE Score

O.3 Admission to the branch of study shall be as decided during CCMT counselling.

O.4 The exact eligibility criteria for admission to the M.Tech programme shall be as approved by the Senate of the Institute from time to time and announced by the Institute on an annual basis.

O.5 The duration of the M.Tech programme will normally comprise of a total of four semesters, including project work.

O.6 Candidates may be permitted to do their project work in industry and other approved organisations as prescribed in the regulations.

O.7 The award of Half-time Teaching Assistantship (HTTA) to the candidates admitted to the M.Tech programme shall be in accordance with the regulations of the Senate of the Institute.

O.8 The award of the M.Tech degree shall be in accordance with the regulations of the Senate of the Institute.

REGULATIONS

R.1.0 ADMISSION

R.1.1 The number of seats in each programme for which admission is to be made in the Institute will be decided by its Senate. Seats are reserved for candidates belonging to the Scheduled Castes, Scheduled Tribes, Other backward classes, Economically weaker sections and physically challenged candidates as per the Government of India orders issued from time to time.

R.1.2 Admission to the M.Tech programme in any year will be based on performance in GATE through a conselling conducted by CCMT.

R.1.3 The students admitted into this programme are required to do a minimum of 8 hours work, such as hanlding theory or laboratory classes, tutorials, Assignments, etc.

R.1.4 Foreign nationals whose applications are received through Indian Council of Cultural Relations, Government of India, are also eligible. Foreign Nationals are also eligible under self-financing scheme for which applications are invited through their embassy.

R.1.5 The eligibility criteria for admission including the minimum GATE score required for admission as full time students with HTTA, will be decided by the Senate.

R.1.6 **T**he conditions for admission to M Tech programmes in IIITDM Kurnool wil be given in the CCMT and Institute websites. However, if at any time the Dean(Academic)/Faculty in-charge(Academic)/ Director finds any of the requirements not fulfilled by the candidate, the Dean(Aacdemic)/ Faculty in-charge(Academic)/ Director may revoke his/her admission to the programme.

R.2.0 STRUCTURE OF THE M.TECH PROGRAMME

R.2.1 The programme of instruction for each stream of specialization will consist of

i. core courses (compulsory)
ii. elective courses
iii. project work

The student may be required to give one or more seminars and undergo industrial / practical training during the programme.

R.2.2 The complete programme will be of 4 semester duration. The academic programmes in each semester may consist of course work and/or project work as specified by the Senate for each specialisation. The total contact hours is normally about 32 hours per week.

R.2.3. Every stream of specialisation in the programme will have a curriculum and syllabi for the courses approved by the Senate. The curriculum is so framed such that the minimum number of credits for successful completion of the M.Tech programme of any stream is not less than 67 and not more than 70.

R.2.4 Credits will be assigned to the courses based on the following general pattern:

i. One credit for each lecture period
ii. Two credits for each laboratory or practical session of three periods
iii. Credits for the seminar, project work and industrial / practical training will be as specified in the curriculum.

R.2.5 A student will have to register for all the core courses listed in the curriculum of his/her selected area of specialisation and successfully complete all of them. However, the Departmental Post Graduate Committee may grant permission to a student not to register for some of the core courses and substitute them by some other courses depending on the courses successfully completed by the student in the undergraduate programme. This has to be intimated to and approved by the Dean (Academic)/Faculty In-charge(Aacdemic) / Director.

R.2.6 Electives will have to be taken from the courses offered by the Department in that particular semester from among the list of approved courses. However, most of the departments permit selection of electives other than those listed against the Department provided they have relevance to the area of specialisation and subject to the approval of the Faculty Adviser.

R.2.7 In some specialisations students may be permitted to register for a maximum of two B.Tech courses. The concerned departments will identify such courses and get prior approval of the Senate.

R.2.8 The medium of instruction, examination, seminar and project reports will be in English.

R.3.0 Faculty Adviser

R.3.1 To help the students in planning their courses of study and for getting general advice on academic programme, the concerned Department will assign a faculty advisor for each M.Tech programme offered in the department in the beginning of every semester.

R.4.0 Class Committee

R.4.1 Every class of the M.Tech programme will have a Class Committee (CC) consisting of Faculty and students.

R.4.2 The constitution of the Class Committee will be as follows:

i) One professor/Head of the department not associated with teaching the class to be nominated by Director to act as the Chairman of the Class Committee.
ii) All faculty teaching the theory /laboratory courses for that class.
iii) Two students from the respective class; and
iv) Faculty Adviser of the respective class.

R.4.3 The basic responsibilities of the class committee are :

a) to review periodically the progress of the classes and discuss issues faced by

students.

b) The type of assessment for the course will be decided by the teacher in consultation with the class committee and will be announced to the students at the beginning of the semester.

c) Each class committee will communicate its recommendations to the Head of the Department and the Dean (Academic)/Faculty In-charge(Academic).

d) The class committee without the student members will also be responsible for the finalisation of the semester results.

R. 4.4 The class committee shall meet at least twice in a semster, once at the beginning of the semester and once before commencment of minor II.

R.5.0 Change of Branch

Change of Programme is not permitted once a student is given admission to M.Tech programme.

R.6.0 Registration Requirement

R.6.1 Except for the First semester, registrarion for the semester will be done during a specified week before starting of that semester. Late registration/enrollment will be permitted with a fine as decided by from time to time up to 2 weeks from the last date specified for regsitration.

R.6.2 The M.Tech students are eligible to take extra courses apart from the courses prescribed in the curriculum, namely, one course in 3rd semester and not more than two courses in 4th semester, subject to a maximum of 9 credits, provided a student has no backlog and should have earned CGPA of 7.0 & above by the end of the previous semester. Students taking extra courses should obtain the prior approval of Dean (Academic)/Faculty In-charge(Academic).

R.6.3 During the final project semester, students are not normally permitted to register for courses. However, students who are short of a few credits required for the degree may be allowed by the Dean (Aacdemic)/Faculty In-charge(Academic) to register for one or two courses along with the project under the specific recommendation from the Head of the department.

In such cases the project duration may have to be extended beyond the normal period suitably. However, the M.Tech HTTA will be paid for a maximum period of 24 months only, as per the existing Government of India rules.

R.6.4 Withdrawal from a course registered is permitted upto two weeks from the date of commencement of the semester. Substitution by another course is not permitted. Courses withdrawn will have to be taken when they are offered next, if they belong to the list of core courses (Compulsory courses).

R.6.5 In extraordinary circumstances like medical grounds, a student may be permitted by the Dean (Academic)/Faculty Incharge(Academic) to withdraw from a semester completely. Normally a student will be permitted to withdraw from the programme only for a maximum continuous period of two semesters.

R.7.0 MINIMUM REQUIREMENT TO CONTINUE THE PROGRAMME

R.7.1 A student should have earned not less than 10 credits in the first semester, 26 credits by the end of second semester and 36 credits by the end of third semester. The student will be asked to leave the programme failing to satisfy this requirement.

R.7.2 In addition to the above, to be eligible to continue in the programme the student should have a minimum CGPA of 5.0, calculated according to the formula in R.23.2. However, in calculating the CGPA for eligibility to continue the programme, only courses the student has successfully completed upto the point under consideration will be taken into account. If the CGPA of any student so calculated falls below 5.0, the student will be issued a warning and if he/she does not make good and get a CGPA less than 5.0 in the following semester also then he/she will be asked to leave the programme.

R.8.0 MAXIMUM DURATION OF THE PROGRAMME

R.8.1 A student is ordinarily expected to complete the M.Tech programme in four semesters. However students who do not complete their project work in third/four semesters, are permitted to submit the report in the fifth semester with the prior approval.

Students should complete the course work in not more than 5 semesters and the entire programme in 8 semesters including the project work from the date of admission to the programme.

R.9.0 DISCONTINUATION FROM THE PROGRAMME

R.9.1 Students may be permitted to discontinue the programme and take up a job provided they have completed all the course work. The project work can be done during a later period either in the organisation where they work if it has R and D facility, or in the Institute. Such students should complete the project within six semesters from the date of admission to the programme.

Students desirous of discontinuing their programme at any stage with the intention of completing the project work at a later date should seek and obtain the permission of the Dean(Aacdemic)/Faculty In-charge(Academic)/Director before doing so.

R.10.0 DISCIPLINE

R.10.1 Every student is required to observe discipline and decorous behaviour both

inside and outside the campus and should not indulge in any activity which brings down the prestige of the Institute.

R.10.2 Any act of indiscipline of a student reported to the Dean will be referred to Discipline and Welfare Committee constituted by the Senate from time to time. The Committee will enquire into the charges and recommend suitable punishment if the charges are substantiated. The appropriate committee will consider the recommendation of the Discipline and Welfare Committee and authorize the Dean(Aacdemic)/Faculty in-charge(Academic) to take appropriate action.

R.10.3. **Appeal:** The student may appeal to the Chairman, Senate, whose decision will be final. The Dean(Academic)/Faculty Incharge(Academic) will report the action taken at the next meeting of the Senate.

R. 10.4 Ragging of any form is a criminal and non-bailable offence in our country and current State and Central legislations provide for stringent punishment including imprisonment. Once the involvement of a student in ragging is established, the concerned student will be dismissed from the Institution and will not be admitted into any other Institution. Avenues also exist for collective punishment, if individuals cannot be identified in this inhuman act. Every senior student of the Institute along with the parent shall give an undertaking every year in this regard and this should be submitted at the time of enrolment.

R.11.0 ATTENDANCE

R.11.1 Students are expected to have 100% attendance in a course. However, students with minimum 85% in each course, either theory/practice, will only be allowed to appear in the end semester examinations. Students failing to meet the minimum attendance percentage will have to repeat the course when it is offered next.

R.11.2 Details of attendance shortage of students for each course/practice should be sent to the Dean (Academic) / Faculty in-charge (Aacdemic) through the concerned Head of the Department.

R.12.0 LEAVE RULES

R.12.1 All M.Tech students should apply to the Head of the Department for leave, stating the reasons whenever they are not in a position to attend classes/project work. They will not be eligible for HTTA for the period of absence, if it is unauthorised leave even if they have not fully utilised the eligible leave.

R.12.2 Students are eligible for leave of 30 days in a year which will be regularised @15 days per semester with a provision of carryover from first to second semester and from the third to fourth semester (i.e unutilized leave from the first year cannot be carried over to second year).

The intervening holidays will be treated as part of leave with provision of suffixing and prefixing holidays.

R.13.0 ASSESSMENT PROCEDURE: TESTS AND EXAMINATIONS

R.13.1 For Lecture or / Lecture and Tutorial based subjects, a minimum of two sessional assessments will be made during the semester. The sessional assessment may be in the form of periodical tests, assignments or a combination of both, whichever suits the subject best. The assessment details as decided at the Class Committee will be announced to the students right at the beginning of the semester by the teacher.

R.14.0 END SEMESTER EXAMINATION

R.14.1 There will be one end semester examination of 3 hours duration in each lecture based subject. In case of practice based subjects, a final examination may or may not be conducted. In the case of project, a viva-voce examination will be conducted on the completion of the project work.

R.15.0 PROJECT EVALUATION

R.15.1 Evaluation of Project work will be taken up only after the student completes all the core as well as elective course requirements satisfactorily.

R.16.0 WEIGHTAGE

R.16.1 The following will be the weightages for different subjects.

(a) Lecture or lecture and tutorial based subjects:
Sessional assessment: Minimum of 40%.
End semester examination: Minimum of 40%

(b) Practice based subjects:
Sessional work: 75 to 100%.
Final examination: if held: 25%

R.16.2 The markings for all tests/ tutorial/ assignments (if any), practice work and examinations will be on an absolute basis. The final percentages of marks are calculated in each subject as per the stipulated weightages.

R.17.0 Make-up Examination

R.17.1 Students who have missed sessional assessments on valid reasons should apply

to the Academic section indicating the reasons for the absence and the Faculty Advisor shall consider these requests suitably.

R.17.2 Students who have missed the end semester examinations on valid reasons, should make an application to the Dean (Academic) /Faculty In-charge(Academic) within ten days from the date of the examination missed. Permission to sit for a make-up examination in the subject(s) is given under exceptional circumstances like hospitalisation or accident to the student. A student who misses this make-up examination will not be normally given another make-up examination.

However, in exceptional cases of illness resulting in the students missing a make-up examination, the Dean (Academic) / Faculty In-charge(Academic) in consultation with the Chairman of the Senate may permit the student to appear for a second make-up examination.

R.17.3 For application on medical grounds, students residing in the hostels should produce a Medical Certificate issued by an Institute Medical Officer only.

Students staying outside the campus permanently/temporarily should produce a medical certificates from registered medical practitioners and the same should be forwarded by the parents/guardian for the purpose of make-up examinations.

The Dean (Academic)/ Faculty in-charge(academic) can use his discretion in giving permission to a student to take a make-up examination, recording the reasons for his/her decision.

R.18.0 Subject wise Grading of Students into Categories

R.18.1 Letter Grades

Each student is awarded a final letter grade at the end of the semester in each subject based on his/her semester performance at the end of the semester. The letter grades and the corresponding grade points are as follows.

Grade	**Points**	
S	10	Grade points
A	9	
B	8	
C	7	
D	6	
E	4	
U	0	Unqualified/Failure
W	0	Failure due to insufficient attendance
I	0	Incomplete (Subsequently to be changed into pass (E to S) or U garde in the same semester)

R.18.2 A student is considered to have completed a subject successfully and earned

the credit if he/she secures an overall letter grade other than U or W or I in that subject.

A letter grade U or W in any subject implies failure in that subject. A subject successfully completed cannot be repeated.

R.18.3 Grades are awarded on relative basis.

R.19.0 Method of Awarding Letter Grades

R.19.1 A final meeting of the Class Committee without the student members will be convened within seven days after the last day of the end semester examination. The letter grades to be awarded to the students for different subjects will be finalised at this meeting.

R.19.2 Two copies of the result sheets for each subject containing the final grade and two copies along with absolute marks and final grade should be submitted by the teacher to the concerned Faculty Advisor for further processing.

After finalisation of the grades at the Class Committee Meeting, one copy with absolute marks and one without the absolute marks but having only the grades will be forwarded by the Class Committee Chairman to the Dean (Academic)/Faculty In-charge(Academic).

One copy with absolute marks, the final grade will be sent to the Head of the Department in which the course is offered.

R.20.0 DECLARATION OF RESULTS

R.20.1 The letter grades awarded to the students in each subject will be anounced in the Institute web site soon after the final Class Committee meeting.

R.20.2 **The W grade once awarded stays in the record of the student and is deleted when he/she completes that subject successfully later.** The grade acquired by him/her will be indicated in the grade card of the appropriate semester with an indication of number of attempts made in that course.

R.20.3 **'U' grade obtained by the student will be deleted in the grade card when he/she completes that subject successfully later. Further, the number of attempts made by the student in that course, will be indicated in the grade card.**

R.21.0 RE-EXAMINATION OF ANSWER PAPERS

R 21.1 As a process of learning by students and also to ensure transparency, the answer scripts after correction of class tests, minor (s), assignments etc., will be shown to the students within two weeks from the date of test/examination. The performance of the students in minors will be discussed in the Class Review Committee.

R.21.2 In order to ensure transparency in the evaluation of scripts of end-semester

examination, those answer scripts also shall be shown to the students up to one day before the finalization of grades. Once the Grades are finalized, the student will no longer have any right to verify his/her answer scripts.

R.21.3 The student can appeal to DAAC for any arbitration within 20 days from the date of official publication of results in the Institute Website.

R. 21.4 Disposal of Answer Scripts

Answer scripts related to a course shall be preserved by the faculty for a period of 6 months from the date of anouncement of results. After this period, the same shall be disposed of as scrap by the institute.

R.22.0 COURSE REPETITION

R.22.1 A student securing 'U' or 'W' grade in any core subject has to repeat it compulsorily when offered next.

R.22.2 A student securing 'U' or 'W' grade in any elective subject has to repeat the course when offered next or he/she can register another equivalent elective course in order to get a sucessful grade.

R.23.0 GRADE CARD

R.23.1 The grade card issued at the end of the semester to each student will contain the following:

a. the credits for each course registered for that semester.
b. the letter grade obtained in each course
d. the total number of credits earned by the student upto the end of that semester.
e. the semester grade point average (SGPA) of all the courses taken in that semester.
f. the Cumulative Grade Point Average (CGPA) of all the courses taken form the first semester till the current semester is shown in the final semester grade card.

R.23.2 The Grade Point Average (GPA) will be calculated by the formula.

$$GPA = \frac{\sum_i C_i \times GP}{\sum_i C_i}$$

Where C_i = credit for the course, GP = the grade point obtained for the course and $\Sigma\ C_i$ is sum of credits of the courses that are successfully completed in that semester.

For the cumulative Grade Point Average (CGPA), a similar formula is used except

that the ΣiCi is the sum of credits in all the courses taken in all the semesters completed upto the point of time, including those in which the student has secured U or W grades.

R. 23.3. No class/division/rank will be awarded to the students at the end of the M.Tech programme.

The formula for conversion of CGPA to percentage is **CGPA×10**.

R.24.0 PROJECT WORK IN INDUSTRY OR OTHER ORGANISATION

R.24.1 Students who desire to do their project work in industries/R&D organizations, may be permitted to carry out their project work in such organisations during the third/final semester.

R.24.2 A departmental committee shall examine the requests from such students, and fix:

i. An internal guide (a faculty member of the institute) along with an area of project work and
ii. External guide (Scientists or Engineer in the Industry).

R.24.3 The above details should be submitted to the Dean (Academic)/ Faculty In-charge (Academic) through the Head of the Department for further processing.

R.24.4 The students who are permitted to do the project work in an industry will have to pay the tuition and other fees to the Institute for the third and fourth semester as well.

R.24.5 Students who do their project work in Industry/R&D Organizations, are permitted to draw stipend only from one source.

R.25.0 HALF-TIME TEACHING ASSISTANTSHIP

R.25.1 Students who are qualified for M.Tech admission through valid GATE score and are admitted as full time students of the Institute, will be eligible for the award of the HTTA notified by the Institute from time to time.

R.25.2 Self-financing foreign nationals are not eligible for HTTA.

R.26.0 ELIGIBILITY FOR THE AWARD OF M.TECH DEGREE

R.26.1 A student shall be declared to be eligible for the award of M.Tech degree if he/she has

(1) Registered and successfully completed all the core courses and the project.
(2) Successfully acquired the minimum number of credits prescribed in the curriculum of the given stream within the stipulated time.
(3) No dues to the Institute, Library and Hostels and
(4) No disciplinary action pending against him/her.
(5) For students visiting Universities abroad under Exchange programme the following will be followed for credit transfer:

The credits / grades obtained from the university where the student has done courses will be indicated in the grade card.

Institute transcripts should only indicate the courses, credits and grades completed at IIITDM and the courses and credits (without grades) done in other Universities in a particular semester.

The CGPA calculation based on credits done at Institute alone is to be considered for award of prizes.

The credits earned at Universities abroad will be considered for calculation of minimum required credits for award of degree

R.26.0 The final award of the Degree must be recommended by the Senate and approved by the Board of Governors of the Institute.

R.27.0 POWER TO MODIFY

Notwithstanding all that has been stated above, the Senate has the right to modify any of the regulations from time to time.