Course Title	Course Code	Structure (I-P-C)		
MOSFET Modelling for VLSI Circuits		**3**	**2**	**4**

Pre-requisite, if any: Electronic Devices and Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Model any kind of MOS Devices in 2-D or 3-D
CO2	Relate the models for further inclusion in circuits
CO3	Develop solution to overcome short channel issues
CO4	Develop various compact models appropriate for industry
CO5	Analyse the frequency response of MOS devices.

Syllabus:

Theory:

1. Intuitive analysis of MOS Transistor- Two-Terminal MOS Structure – Flatband Voltage, Surface Condition, General Analysis, Inversion, Strong Inversion, Weak Inversion, Small- Signal Capacitance, Three-Terminal MOS Structure (7 hours)

2. Long-Channel MOS Transistor, Introduction All-Region Models, Strong Inversion Models, Weak Inversion Models, Source Reference vs. Body Reference, Effective Mobility (5 hours)

3. Small-Dimension Effects - Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain-Induced Barrier Lowering, Hot Carrier Effects, Velocity Overshoot Ballistic Operation, Polysilicon Depletion (6 hours)

4. Small-Dimension Effects-Modelling for Circuits Simulation- Quantum-Mechanical Effects; Gate Current, Junction Leakage, Scaling and New Technologies, Approaches, and Properties of Good Models, Model Formulation Considerations, Parameter Extraction, Compact Models, Benchmark Tests (7 hours)

5. Small-Signal Modelling - Conductance Parameter Definitions and Equivalent Circuits, Conductance Parameters Due to Gate and Body Leakage, Transconductance, Source-Drain and Output Conductance, Capacitance Definitions and Equivalent Circuits, Capacitance Evaluation and Properties, y-Parameter Model, RF Models (11 hours)

Practice:

Introduction to Technology computer aided design (TCAD) tools; inputs and outputs of device and process simulations. (8 hours)

2. Device simulation: observing the terminal characteristics and distributions of carriers, current, field, potential and energy band diagrams within the device. (8 hours)

3. Process simulation: observation of device structure and doping profile Simulation of 2-D MOSFETs through device and process simulations (8 hours)

4. Simulation of novel 3-D transistors such as III-V HEMT, LEDs, FinFETs, GAA devices, solar cells etc, through device simulation (8 hours)

5. DC, AC, RF mixed mode and noise simulation for the devices (8 hours)

Text Book(s):

1. Y. Tsividis and C. McAndrew, “MOSFET modelling for Circuit Simulation”, Oxford University Press, 2011

2. C K Maiti, “Introducing Technology Computer-Aided Design (TCAD): Fundamentals, Simulations, and Applications”, Jenny Stanford Publishing; 1st Edition, 2017, ISBN: 978-9814745512.

3. Wu, Yung-Chun, Jhan, Yi-Ruei, “3D TCAD Simulation for CMOS Nanoeletronic Devices", Springer, 2017, ISBN 978-981-10-3066-6

References & Web Resources:

1. T. A. Fjeldly, T. Yetterdal, and M. Shur, “Introduction to Device Modeling and Circuit Simulation”, John Wiley, 1998.

2. Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 1998.

3. Y. P. Tsividis, “Mixed Analog-digital VLSI Devices and Technology”, World Scientific Publishing Co Pte Ltd, 2002

4. C K Sarkar, “Technology Computer Aided Design: Simulation for VLSI MOSFET”, CRC Press, 1st Edition, 2013, ISBN: 978-1466512658.

5. J.-P. Colinge, “FinFETs and Other Multi-Gate Transistors”, Springer, 2008, ISBN: 978- 0-387-71751-7

Course Title	Course Code	Structure (I-P-C)		
Digital VLSI System Design		**3**	**2**	**4**

Pre-requisite, if any: Digital Logic Design, VLSI Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design digital systems using HDL and CMOS transistors.
CO2	Analyse the circuit/system performance, area, and power dissipation
CO3	Implement the low power and high throughput techniques on digital integrated circuits
CO4	Develop the Custom IPs to integrate into Digital Systems
CO5	Design the RTL based digital circuits using HDL.
CO6	Develop the hardware-software co-design using VLSI CAD tool.

Syllabus:

Theory:

1. Introduction to Digital design: timing issues, pipelining, folding/unfolding, resource sharing, metastability, synchronization, clock skew, setup/hold time of flip-flops, synchronization between multiple clock domains using FIFO, PLL, and DLL, reset – recovery/removal time, false path. (5 hours)

2. Digital Systems Design with ASICs: PLDs, Semi/full custom ASIC designs, Emphasis on the synthesis based approach to VLSI Design. Relevant issues related to physical design automation such as partitioning, floor planning, power planning, placement & routing, Algorithms for VLSI Physical Design, IO pads, electro static discharge. (10 hours)

3. Digital Systems Design with FPGAs: Hardware-Software Co-design, Custom IP Development, High level synthesis (HLS), Efficient Coding Techniques in High Level Language for HLS, Partial Reconfiguration. (5 hours)

4. CMOS Transistor Logic: I-V characteristics, Short channel effects, Mobility degradation & velocity saturation, channel length modulation, body effect, drain induced barrier lowering, leakage, RC delay model, logical effort, clock gating, dynamic voltage scaling, power gating, glitch free circuits, dual-edge triggering, static CMOS, ratioed circuits, dynamic CMOS, domino logic, pass transistor logic, (10 hours)

5. CMOS Synchronous Circuits: CMOS latches, CMOS flip flops, dual edge triggered flip flops, synchronizers, arbiters, wave pipelining. (5 hours)

6. Memory Designs: SRAM, DRAM, ROM, PROM, EPROM, EEPROM, Flash, CAM (5 hours)

Practice:

1. Introduction to RTL Design**:** Basic combinational (half adder, full adder, multiplexer, decoder, and so on) and sequential circuits design (Flip-flops and counters) using HDL with commercial VLSI CAD tools or open source compilers. (5 hours)

2. Familiarity of Datapath elements**:** 32-bit Ripple carry adder, recursive doubling based carry look ahead adder, Braun multiplier, Wallace tree multiplier, non restoring based division, IEEE-754 floating point adder/Subtractor/multiplier/divider, CORDIC, modular multiplier, modular multiplicative inverse, modular exponentiation, cross-bar switch, Banyan switch, Batcher switch, digital FIR filter. (10 hours)

3. Advanced VLSI circuit design concepts**:** Pipelining, clock gating to reduce the switching power dissipation, hardware reuse strategy (folded hardware) to reduce the area, fault tolerant digital circuit design, formal hardware verification using equivalence check, high level synthesis with EDA, performance analysis of RTL design & high level synthesis based digital system using EDA, partial reconfiguration using EDA. (5 hours)

4. Hardware-Software Co-design**:** Design flow of hardware-software co-design using FPGA evaluation board with EDA, Custom IP design (arithmetic circuits as mentioned above), hardware-software partitioning, and performance analysis of various hardware-software co-design techniques. (10 hours)

5. Digital Circuits Design using CMOS**:** logic gates, combinational logic circuits, low power CMOS circuits using VLSI CAD tool. (10 hours)

Text Book(s):

1. Neil H.E. Westte and David Money Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley, 4th Edn, 2011.

References & Web Resources:

1. Wakerly, J. F., "Digital Design: Principles and Practices", 4th Edition, Pearson, 2008

2. MironAbramovici, Melvin A Breuer, and Arthur D Friedman, "Digital Systems Testing and Testable Designs", Wiley-IEEE Press, 1994.

3. N. A. Sherwani, "Algorithms for VLSI Physical Design Automation", Bsp Books Pvt. Ltd., 3rd edition, 2005.

4. Samir Palnitkar, "Verilog HDL - Guide to Digital design and synthesis", Pearson Education, 3rd Edn, 2003.

Course Title	Course Code	Structure (I-P-C)		
Embedded System Design		**3**	**2**	**4**

Pre-requisite, if any: Microprocessors and Microcontrollers

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the basic elements of embedded systems such as I/O and interfaces.
CO2	Understand embedded system design using the ARM Cortex-M microcontroller with the Launch pad IDE in C.
CO3	Develop the rapid prototype of embedded systems using microcontrollers.
CO4	Build wireless networked embedded systems using Arduino shields and modules (e.g., GPS, GSM/GPRS, Bluetooth, RFID, and ZigBee).
CO5	Exploit the advanced concepts such as networking and wireless communications, real-time operating systems and control, and Internet of Things in the real time embedded systems.
CO6	Develop the hardware-software co-design with parallel threads
CO7	Conduct experiments in Internet of Things

Syllabus:

Theory

1. Introduction to Embedded Systems: Elements of embedded systems (such as microcontrollers, GPIO, communication, interrupts, ADC, and DAC); overview of microcontroller; Comparison between Hardware, Software, and Firmware; Comparison between Hard, Soft, Firm, and Hybrid real time systems; applications of embedded systems; classification of embedded systems; characteristics of embedded systems; hardware-software partitioning; (5 hours)

2. RTOS: Software aspects of embedded systems; Real-time operating system (RTOS) - mutual exclusion using semaphore; deadlock; critical section; event-driven scheduling; time sharing; earliest deadline first scheduling; pre-emptive scheduling; non-pre-emptive scheduling; multi-tasking; multi-threading; inter-process communication using mboxes, and pipes; priority inversion; (10 hours)

3. Prototyping: Rapid prototyping of embedded systems with advanced microcontroller boards; (5 hours)

4. IoT: Basic elements of IoT; IoT systems design using advanced microcontroller boards; (10 hours)

5. Communication Protocols: I2C, CAN, PCIe, SPI, UART, USB (10 hours)

Practice

1. Experiments in GPIO such as switches, LEDs, LCD, Key pad, Seven Segment Display, Buzzer, and relay; (5 hours)

2. Serial and parallel interfacing; data acquisition with ADC, audio, and video; timer interrupts; Various bus inter connects such as I2C, UART, SPI, and so on; (5 hours)

3. DAC Experiments in control of RC servos, stepper motors, and DC motors; (5 hours)

4. Data acquisition and real-time control with uC boards, FPGA boards; (5 hours)

5. Add-on boards Experiments in wireless networked systems with GPS, GSM/GPRS, ZigBee, Bluetooth, and RFID; (5 hours)

6. Hardware-software co-design experiments using FPGA boards. (5 hours)

7. Experiments in IoT for smart automation using sensors, microcontrollers, and cloud. (5 hours)

8. Free RTOS based applications and PSoC trainer board based experiments. (8 hours)

Text Book(s):

1. D. Gajski, F. Vahid, S. Narayan, and J. Gong. “Specification and Design of Embedded Systems”, Prentice Hall.

References & Web Resources:

1. J. W. Valavano, “Embedded Systems: Introduction to Arm Cortex-M Microcontrollers", 2nd edition, Create Space, 2012. ISBN: 978-1477508992.

2. J. W. Valavano, “Embedded Systems (Vol-2): Real-Time Interfacing to ARM Cortex-M Microcontrollers", 2nd edition, Create Space, 2011, ISBN: 978-1463590154.

3. J. W. Valavano, “Embedded Systems (Vol-3): Real-Time Operating Systems for Arm Cortex M Microcontrollers", 2nd edition, Create Space, 2012. ISBN: 978-1466468863.

4. A. McEwen and H. Cassimally, “Designing the Internet of Things”, 1st edition, Wiley, 2013. ISBN: 978-8126556861.

Course Title	Course Code	Structure (I-P-C)		
Analog VLSI design		**3**	**2**	**4**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Analyse effect of mismatch between components in the performance of ICs
CO2	Model MOSFET in IC
CO3	Analyse noise in different components in the IC
CO4	Derive the Data Sheet / Specifications of Single stage, two stage, folded cascode op amps
CO5	Understand fully differential operation, opamp and make such circuits

Syllabus:

Theory

1. Introduction of CMOS technology: Components and mismatch in CMOS process, models and Layout techniques. (4 hours)

2. MOS Transistor: Layout, model, Body effect, transit frequency. (4 hours)

3. Small signal analysis: Small signal analysis of MOSFET based amplifiers, cascade and cascode MOSFET based amplifiers (10 hours)

4. Noise: Noise in Resistor, capacitor, and MOSFET, spectral density (4 hours)

5. Differential amplifiers, current mirror, cascode current mirror, folded cascodemulti stage, and Miller compensated op amps. (6 hours)

6. Single stage op amp: Noise, offset, swing limits and slew rate, Loop gain and stability Analysis in two and higher order opamp (5 hours)

7. Operational amplifiers based circuits: arithmetic circuits, oscillators, active filters. (10 hours)

8. PLL (5 hours)

Practice

1. Design of MOSFET based amplifiers: Schematic and layout simulation using EDA tools (15 hours)
2. Design of Op Amp based Circuits: Schematic and layout simulation using EDA tools (15 hours)

Text Book(s):

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd edition McGraw-Hill Education, 2016, ISBN: 978-0-07-252493-2

2. Baker, R. Jacob, "CMOS: Circuit design, Layout, and Simulation", John Wiley & Sons, 2019.

References & Web Resources:

1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, Inc., 2012, ISBN: 978-0-470-77010-8.

2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, “Analysis and Design Of Analog Integrated Circuits”, 5th edition, John Wiley & Sons, Inc., 2009. ISBN: 978-0- 470-24599-6.

3. TertulienNdjountche, “CMOS Analog Integrated Circuits High-Speed and PowerEfficient Design”, CRC Press Taylor & Francis Group, 2011. ISBN: 978-1-4398- 5500-3

Course Title	Course Code	Structure (I-P-C)		
Advanced Computer Architecture		**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Circuits, Microprocessors and Microcontrollers

Course Outcomes: At the end of the course, the students will be able to:

CO1	Interpret the performance of a processor based on metrics such as execution time, cycles per instruction (CPI), Instruction count etc
CO2	Predict the challenges of realizing different kinds of parallelism (such as instruction, data, thread, core level) and leverage them for performance advancement
CO3	Apply the concept of memory hierarchy for efficient memory design and virtual memory to overcome the memory wall
CO4	Explore emerging computing trends, computing platforms, and design trade-offs Teaching Methodology
CO5	Design a data path of Harvard processor.

Syllabus:

Theory

1. Design Space Exploration and Optimizations: Performance metrics and performance enhancement techniques, basic concepts of parallel processing and pipelining, power dissipation in processors, power metrics, low-power design techniques, and Amdhal's law (5 hours)

2. Instruction set architecture design: Instruction set design, implementation and performance perspectives, relative advantages of RISC and CISC instruction set, processor datapath design using Von Neumann and Harvard architectures. (5 hours)

3. Instruction-level parallelism (ILP): Pipeline data-path, data-dependence. challenges in ILP realization. instruction hazards and their solutions, out-of-order execution, control hazards, branch prediction, VLIW and superscalar processors, control hazards, static and dynamic prediction, dynamic instruction scheduling using score board, Thomosulo engine, and hardware speculation. (10 hours)

4. Memory systems: Brief overview of memory technologies (SRAM, DRAM, ROM, CAM, and flash), overview of memory hierarchy, cache design considerations, instruction vs. data caches, read, write, and replacement policies in cache, analysis of cache performance, and cache design for performance enhancement, cache coherence protocols, virtual memory organization. (10 hours)

5. Data Level Parallelism: Flynn's processor classification, SIMD, MIMD, GPU architectures (5 hours)

6. Multicore implementations: tightly and loosely coupled multicore architectures (5 hours)

Practice

1. Processor data path design (Harvard Architecture with Microprogramming based Controller) in HDL: It includes the functional units such as logic unit, fixed/floating point adder, multiplier, and divider. Here, two separate memories are used for data and instruction. (15 hours)

2. Implementation of ILP and DLP processors: dynamic instruction scheduling, hazard resolution techniques (15 hours)

3. Memory Design: cache memory design, cache coherence protocol design (5 hours)

Text Book(s):

1. J .L. Hennessy, D.A.Patterson, “Computer Architecture: a quantitative approach”, Morgan Kaufmann, 5th edition, 2011, ISBN: 978-1558605961.
2. William Stallings, “Computer Organization and Architecture”, Prentice Hall, 10th edition, 2015, ISBN-10: 013293633X, ISBN-13: 978-0132936330

References & Web Resources:

1. David E. Culler, Jaswinder Singh, and Morgan Kaufmann, “Parallel Computer Architecture: A Hardware/ Software Approach”, MK Publishers
2. C. Hamacher, Z. Vranesic and S. Zaky, “Computer Organization”, McGraw-Hill, 5th edition,2002, ISBN: 0072320869.
3. Andrew S. Tanenbaum, “Structured Computer Organization”, Prentice Hall, 6th edition, 2012, ISBN: 978-0132916523.
4. J.P. Shen and M.H. Lipasti, “Modern Processor Design", MCGraw Hill, Crowfordsville, 2005
5. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill

Course Title	Course Code	Structure (I-P-C)		
Digital Signal Processing and Architectures		**3**	**2**	**4**

Pre-requisite, if any: Digital Signal Processing, Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concepts of digital signal processing: Filtering Techniques and Orthogonal Transformations.
CO2	Develop the hardware designs of various Digital Filtering
CO3	Develop the hardware designs of various Orthogonal Transformations
CO4	Design the co-processor for digital signal processing
CO5	Analyse the multi rate signal processing

Syllabus:

Theory

1. Digital filter design: Basics of folded/parallel design, FIR/IIR filter design, steepest- descent LMS algorithm, adaptive FIR filter design, multirate signal processing, polyphase decomposition, and filter banks. (15 hours)

2. Discrete wavelet transform: Haar wavelet, 1D/2D/3D-Convolution based discrete wavelet transform architecture, 1D/2D/3D-(5,3) and (9,7) lifting based discrete wavelet transform architecture. (10 hours)

3. FFT architectures: radix-2/4 SDF, MDC, parallel FFT architectures. (5 hours)

4. HEVC architectures: introduction to DCT, integer DCT architectures, and discrete Hadamard transform architectures. (5 hours)

5. Motion Picture Estimation: Algorithms on motion picture estimation (5 hours)

Practice

1. Hardware/software co-design of signal processing operations (8 hours)
2. Digital Signal Co-processor design (8 hours)
3. Digital Filter Designs – FIR, IIR, Adaptive filters (8 hours)
4. Discrete Orthogonal Transform Designs – FFT, integer DCT, DHT, DWT (8 hours)
5. Experiments using DSP trainer kits (8 hours)

Text Book(s):

1. S. K. Mitra, "Digital Signal Processing: A computer base approach", Third edition, McGraw Hill Higher Education, 2006.
2. Y.T. Chan, "Wavelet Basics", Kluwer Publishers, Boston, 1993.
3. Simon Haykin, "Adaptive filter theory", Pearson Education, Fifth edition, 2014.

References & Web Resources:

1. V. Oppenheium and R. W. Schafer, "Discrete-time signal processing", Second edition, Prentice Hall, 1999.

Course Title	Course Code	Structure (I-P-C)		
Mixed Signal Integrated Circuits		**3**	**2**	**4**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze ADC and DAC using EDA tools
CO2	Apply the concepts for mixed signal MOS circuit
CO3	Analyze the signal to noise ratio and modeling of mixed signals
CO4	Understand the characteristics of ADC and DAC
CO5	Design ADC and DAC using full custom ASIC

Syllabus:

Theory

1. Data converter fundamentals: Analog versus digital (or discrete time) signals, converting analog signals to data signals, sample and hold circuits, sample and hold characteristics, switched capacitor circuits, DAC specifications, ADC specifications.

2. Sample and hold and trans-linear circuits: Performance of sample-and-hold circuits – testing sample and holds, MOS sample-and-hold basics, examples of CMOS S/H Circuits, bipolar and BiCMOS Sample-and-Holds, Translinear gain Cell, trans-linear multiplier

3. DAC architectures: digital input code, R-2R ladder networks, current steering, charge scaling DACs, cyclic DAC, pipeline DAC.

4. ADC architectures: flash ADC, 2-step flash ADC, pipeline ADC, integrating ADC, successive approximation ADC.

5. Oversampling ADCs

Practice

1. Design and analysis of DACs in VLSI CAD tools (20 hours)

2. Design and analysis of ADCs in VLSI CAD tools (20 hours)

Text Book(s):

1. Baker, R. Jacob, "CMOS: Mixed Signal Circuit Design", John Wiley & Sons, 2019.

2. Behzad Razavi, "Principles of Data Conversion System Design", Wiley

References & Web Resources:

1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, "Analog Integrated Circuit Design", John Wiley & Sons

2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd edition McGraw-Hill Education, 2016

Course Title	Course Code	Structure (I-P-C)		
VLSI Verification and Testing		**3**	**2**	**4**

Pre-requisite, if any: Digital Logic Circuits, VLSI Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyse complex VLSI systems using industry level Design and verification tools.
CO2	Understand the concept of yield and identify the parameters influencing the same
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Syllabus:

Theory

1. Formal Hardware Verification: equivalence check and model check algorithms, compiler optimizations for formal verification, temporal logic, binary decision diagrams: OBDD, ROBDD, and BMD. (10 hours)

2. Introduction to VLSI Testing: Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. (3 hours)

3. Fault Modelling: Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. (4 hours)

4. Automatic Test Pattern Generation: Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design. (8 hours)

5. DFT, scan chains, and BIST: Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, Boundary scan testing. (8 hours)

6. Memory and Delay Test: Testable memory design-Test algorithms-Test generation for Embedded RAMs, hazard free, robust, and non robust path delay fault tests, transition delay fault test. (8 hours)

7. Test Compression: Test Data Compression, Compression Methods and Decompression Methods. (4 hours)

Practice

1. Formal Verification: Basic UVM constructs & classes, design a basic test environment using UVM, System Verilog/HDL verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification. (20 hours)

2. VLSI Testing: Verify fault coverage of test patterns, simulate fault, apply test pattern, and observe output, Hands-on on Design for test (DFT) – insert test points, scan chains, to improve

testability, Writing ATPG and Designs for Combinational and Sequential Circuits, Design of LFSR for BIST, Fault Models simulations and verifications, Structural Testing with Fault Models, and Implement path delay fault testing. (20 hours)

Text Book(s):

1. ZainalabedinNavabi, “Digital System Test and Testable Design using HDL Models and Architecture”, 1st edition, Springer, 2010, ISBN: 978-1-4419-7547-8

2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSICircuits”, Springer, 2004. ISBN: 7923- 7991-8.

3. SystemVerilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling, 2 nd Edition, ISBN-13: 978-0387333991

4.Erik Seligman, Tom Schubert, andM V Achutha Kiran Kumar, “Formal Verification: An Essential Toolkit for Modern VLSI Design”, MK Publishers.

References & Web Resources:

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press.

2. Chris Spear, “SystemVerilog for Verification: A Guide to Learning the Testbench Language Features", Springer. 2012, ISBBN: 978-1461407140.

3. Donald Thomas, Logic Design and Verification Using SystemVerilog, 2016, ISBN: 1523364025.

4. “UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology”, 2013, ISBN: 0974164933.

Course Title	Course Code	Structure (I-P-C)		
RFIC Design		**3**	**0**	**3**

Pre-requisite, if any: Engineering Electromagnetics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Analyze RF frequency filters, couplers, amplifier, oscillators and mixer circuits and LNA.
CO2	Design RF frequency filters, couplers, amplifiers, and LNA.
CO3	Design Oscillators, mixers and Phase Locked Loops
CO4	Develop RFICs.

Syllabus:

Introduction to RF and Wireless Technology: A Wireless World, RF Design Is Challenging, The Big Picture, Basic concepts in RF Design, General Considerations, Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation, Scattering Parameters, Analysis of Nonlinear Dynamic Systems, Volterra Series.

Communication Concepts: General Considerations, Analog Modulation, Digital Modulation, Spectral Regrowth, Mobile RF Communications, Multiple Access Techniques, Wireless Standards.

Transceiver Architectures: General Considerations, Receiver Architectures, Transmitter Architectures.

Low Noise Amplifiers and Mixer Design: General Considerations, Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs, Nonlinearity Calculations, General Considerations of Mixer, Passive Downconversion Mixers, Active Downconversion Mixers, Improved Mixer Topologies, Upconversion Mixers.

Passive Devices: General Considerations, Inductors, Transformers, Transmission Lines, Constant Capacitors.

Oscillators and Phase Locked Loop: Performance Parameters, Basic Principles, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators, Tuning Range Limitations, LC VCOs with Wide Tuning Range, Phase Noise, Low-Noise VCOs, LO Interface, Mathematical Model of VCOs, Quadrature Oscillators, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase Noise in PLLs, Loop Bandwidth, Design Procedure.

Basics of Integer-N Frequency Synthesizers, Fractional-N Synthesizers and power Amplifiers, Transceiver Design Example.

Text Book(s):

1. Behzad Razavi, RF Microelectronics, 2nd Edition, Pearson, 2011.

References & Web Resources:

1. I.D. Robertson , S. Lucyszyn, RFIC and MMIC Design and Technology: 13 (Materials, Circuits and Devices), Institution of Engineering and Technology, 2001.

Course Title	Course Code	Structure (I-P-C)		
Electronic Packaging and Manufacturing		**3**	**2**	**4**

Pre-requisite, if any: Basics of Electrical & Electronics Engineering

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understands the electronics packaging including package styles or forms, hierarchy and methods of packaging necessary for various environments.
CO2	Provides industry perspective in the electronics packaging
CO3	Ability to distinguish between engineering performance and economic considerations to develop cost-efficient and high performance packaging approaches.
CO4	Predict the reliability of electronic components and structures.
CO4	Implementation of PCB design with different application

Syllabus:

Theory

1. Overview of Electronic Systems Packaging: Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products, Definition of PWB, Basics of Semiconductor and Process flowchart, Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire bonding, TAB and flip chip. (8 hours)

2. Electronic systems and needs, physical integration of circuits, packages, boards and complete electronic systems; system applications like computer, automobile, medical and consumer electronics with case studies and packaging levels. (8 hours)

3. Electrical design considerations - power distribution, signal integrity, RF package design and Power-delivery in systems. CAD for Printed Wiring Boards (PWBs) and Design for Manufacturability (DFM). PWB Technologies, Single-chip (SCM) and Multi-chip modules (MCM), flex circuits. Recent trends in manufacturing like microvias, sequential build-up circuits and high-density interconnect structures. (8 hours)

4. Materials and processes in electronics packaging, joining methods in electronics; lead-free solders. Surface Mount Technology - design, fabrication and assembly, embedded passive components. (8 hours)

5. Thermal management of IC and PWBs, Cooling Requirements, Electronic cooling methods thermo-mechanical reliability, design for reliability, electrical test and green packaging issues, Design for Reliability – Fundamentals, Induced failures. Electrical Testing –System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability. Trends in packaging. (8 hours)

Practice

1. PCB design flow- Schematic -layout - PCB design using created library - PCB printing using PCB prototyping machine-Testing and debugging of PCB. (4 hours)

2. Familiarization of different components and chip packages. (4 hours)

3. PCB Design for manufacturability. (4 hours)

4. PCB Design consideration for special circuits. (4 hours)

5. Design and development of PCBs using different simulator tools and prototyping. (4 hours)

6. Hands-on lab sessions for board manufacturing and assembly. (4 hours)

7. Thermal and Heat Sink Design. (4 hours)

8. Electrical Testing and Active Circuit Testing. (4 hours)

Text Book(s):

1. Rao R. Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001

2. Rao R Tummala and Madhavan Swaminathan, “Introduction to System-on-Package”, McGraw Hill, 2008

3. R S Khandpur,” Printed Circuit Boards”, McGraw Hill, 2006

4.Richard K. Ulrich and William D. Brown, “Advanced Electronic Packaging”, 2nd Edition :IEEEPress, 2006

References & Web Resources:

1. Jan Axelson, “Making Printed Circuit Boards”, TAB/McGraw Hill, 1993
2. Ronald A. Reis, “Electronic project design and fabrication”, 6/E, Prentice Hall, 2005.

Course Title	Course Code	Structure (I-P-C)		
Analog and Mixed Signal Circuit Design		**3**	**0**	**3**

Pre-requisite, if any: Analog Electronics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze complex analog integrated circuits using industry level analog IC Design tools
CO2	Design and analyze ADC and DAC using EDA tools
CO3	Design and analyze various MOSFET based arithmetic circuits.
CO4	Learn the various methods of power optimization in analog circuits.
CO5	Learn various circuits of design of Operational Amplifier

Syllabus:

Introduction: Review of single state MOS amplifiers, current mirrors, cascode current mirrors, active current mirrors, biasing techniques.

Op-amp design: Differential pair with current mirror load, single stage op-amp characteristics, single stage op-amp tradeoffs, telescopic cascode op-amp, folded cascode op-amp, two stage op-amp, fully differential single stage op-amp.

Data converter fundamentals: Analog versus digital (or discrete time) signals, converting analog signals to data signals, sample and hold circuits, sample and hold characteristics, switched capacitor circuits, DAC specifications, ADC specifications.

Data converters: DAC architectures – digital input code, R-2R ladder networks, current steering, charge scaling DACs, cyclic DAC, pipeline DAC, ADC architectures – flash ADC, 2-step flash ADC, pipeline ADC, integrating ADC, successive approximation ADC.

Phase locked loop: simple PLL, frequency/phase detectors, charge pump PLL, application as frequency multiplier.

Text Book(s):

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill International Edition 2016.
2. Baker, R. Jacob, CMOS: Circuit design, Layout, and Simulation. John Wiley & Sons, 2019.

References & Web Resources:

1. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2003.
2. Behzad Razavi, Fundamentals of Microelectronics, Second edition, Wiley, 2013
3. P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis And Design Of Analog Integrated Circuits, 5th edition, John Wiley & Sons, Inc., 2009.

Course Title	Course Code	Structure (I-P-C)		
Artificial Intelligence and Machine Learning		**3**	**0**	**3**

Pre-requisite, if any: Linear Algebra, Probability Theory, and Statistics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the applications of Linear Algebra and Probability in Machine Learning
CO2	Familiarize with traditional and modern learning paradigms with their applications in the real-world systems
CO3	Adapt human training for the development of intelligent machines
CO4	Model any real-world practical problem in a machine-learning domain
CO5	Grasp the artificial neural networks with an understanding of the modern deep-learning techniques

Syllabus:

Introduction to machine learning: learning systems, classification, clustering, regression, separability of problems; introduction to learning paradigms: supervised, unsupervised, semi supervised, active, reinforcement with examples; cross-validation; performance evaluation metrics for classification and clustering; curse of dimensionality, feature selection, reduction and expansion, computation of Eigen co-ordinates and principle component analysis.

Recognition systems and design cycle, Non-linearly separable problems: solutions through Cover's theorem with examples, parametric learning mechanisms like Maximum likelihood, expectation maximisation, aposteriori probabilities, Instance-based learning, Lazy learning with K-nearest neighbour, Eager learning with basis functions, non-parametric learning using support vector machines (SVMs).

Artificial neural networks: Analogy of biological neural network with artificial neural network; Perceptron learning; gradient descent algorithm; multi-layer perceptrons; backpropagation algorithm; activation functions, delta rule, learning curves: overfitting and underfitting of models; Hebbian learning, self-organising feature map, radial basis function neural networks.

Deep neural networks: Introduction and advent of deep learning paradigm, solutions to vanishing and exploding gradient problems, regularisation, activation functions for deep learning, deep feed forward network, convolutional neural network (CNN), pretrained CNN models, attention network, generative models like auto-encoders and adversarial learning, recurrent neural networks, problem solving through deep learning and open areas of research**.**

Text Book(s):

1. T. M. Mitchell, Machine Learning, McGraw-Hill, 1997.
2. S. Haykin, Neural Networks: A Comprehensive Foundation. Prentice-Hall of India, 2007.

Reference Book(s):

1. R. O. Duda, P.E. Hart, D. G. Stork, Pattern Classification, John Wiley, 2001
2. I. Goodfellow, Y. Bengio, and A. Courville, Deep Learning, MIT Press, 2016

Course Title	Course Code	Structure (I-P-C)		
Circuits for Electronic System Design		**3**	**0**	**3**

Pre-requisite, if any: Analog Electronics and Digital Logic Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Apply concepts of Analog circuits for signal conditioning, signal processing, controller circuits, and driver circuits for power electronic circuits.
CO2	Design transformer and different power sources for various applications
CO3	Understand the interface of various modules to microcontroller and learn various communication protocols
CO4	Perform descriptive error analysis for the circuits
CO5	Demonstrate key concepts in electronics circuit design, including tools, approaches, and application scenarios

Syllabus:

1. Introduction to Op-Amps: Op-amp Characteristics, Negative feedback, Gain of the Op-Amp
2. Analog Signal conditioning circuits**:** Buffering, scaling, level translation, filtering applications, Analog math circuits - arithmetic circuits, log circuits, trigonometric circuits and applications Timer circuits, pulse width modulation circuits, P, PI and PID controller circuits, protection circuits, base and gate drive circuits for power transistors, MOSFETs and IGBTs, relay and contactor drive circuits. Design and error budget analysis of signal conditioners for low level AC and DC applications. Error Analysis.
3. Power supply circuits:Board level power supply circuits to generate +/-12V, 5V, 3.3V, 1.8V. Linear regulators, low drop out regulators, charge pumps, switched mode power converters.
4. Interfacing circuits**:** A to D, D to A, A to A and D to D interfaces, serial and parallel DACs, sampling, RS-232, USB, I2C, LCD, serial memory, SPI, CAN, wireless (RF, WiFi) Ethernet, RFID, SD card, SIM card, GPS, Touchscreen interfaces.

Digital circuit essentials**:**Digital filters, moving average, numeric formats, scaling, normalizing, arithmetic, log, exponential, square root, cube root, hypotenuse, sine, 3 phase waves, PWM etc.

References & Web Resources:

1. Franco, S., Design with operational amplifiers and analog integrated circuits. Mc. Graw Hillbook Co. 1988.
2. Horowitz, P., and Hill, W., The art of electronics (2nd edition), Cambridge University Press. 1992.
3. Abraham Pressman, Keith Billings, Taylor Morey, Switching Power Supply Design, McGraw-Hill Education, 2009
4. Warwick A. Smith, ARM Microcontroller Interfacing: Hardware and Software, Elektor Electronics Publishing, 2010
5. Datasheets and Application notes of different Integrated circuits.

Course Title	Course Code	Structure (I-P-C)		
Cognitive Communication Networks		**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the Cognitive Communication and networking as per applications.
CO2	Detects the desired signal in the scrambled spectrum.
CO3	Understand algorithms for cognitive networks.
CO4	Understand the MAC protocols in cognitive networks.

Syllabus:

Introduction to Cognitive Radio: Introduction –Software Defined Radio: Architecture–Digital Signal Processor and SDR Baseband architecture – Reconfigurable Wireless Communication Systems – Digital Radio Processing –Cognitive Radio: Cognitive radio Framework – Functions – Paradigms of Cognitive Radio.

Spectrum Sensing: Introduction –Spectrum Sensing – Multiband Spectrum Sensing – Sensing Techniques – Other algorithms – Comparison – Performance Measure & Design Trade-Offs: Receiver operating characteristics – Throughput Performance measure –Fundamental limits and trade-offs.

Cooperative Spectrum Acquisition: Basics of cooperative spectrum sensing–Examples of spectrum acquisition techniques – cooperative transmission techniques – sensing strategies– Acquisition in the Presence of Interference: Chase combining HARQ –Regenerative cooperative Diversity– spectrum overlay– spectrum handoff.

MAC Protocols and Network Layer Design: Functionality of MAC protocol in spectrum access – classification –Interframe spacing and MAC challenges – QOS – Spectrum sharing in CRAHN – CRAHN models – CSMA/CA based MAC protocols for CRAHN – Routing in CRN– Centralized and Distributed protocols – Geographical Protocol.

Text Book(s):

1. Mohamed Ibnkahla, “Cooperative Cognitive Radio Networks:The complete Spectrum Cycle” I edition.
2. Ahamed Khattab, Dmitri Perkins,BagdyByoumi,“Cognitive Radio Networks from Theory to Practice " 2013th edition.

References & Web Resources:

1. Kwang-Cheng Chen and Ramjee Prasad, “Cognitive Radio Networks, Wiley Publications
2. Alexander M.Wyglinski,MaziarNekovee, ThomasHou,” Cognitive Radio Communications and Networks”. I edition.

Course Title	Course Code	Structure (I-P-C)		
Communication Protocols for Electronic System Design		**3**	**0**	**3**

Pre-requisite, if any: NIL

Course Aim: To teach fundamentals of communication protocols for designing electronic systems.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Quantitative analysis of individual components of industrial data communications.
CO2	Analysis and specification of serial communication protocol standards.
CO3	Understanding the error detection, cable shielding techniques to avoid stray pickups, noise.
CO4	Systematic understanding and development of industrial communication protocols.
CO5	Implement the different communication protocols for different applications

Syllabus:

Overview: Standards, OSI model, Protocols, Physical standards, Modern instrumentation and control systems, PLCs, Smart instrumentation systems, Communication principles and modes, error detection, Transmission, UART.

Serial communication standards: Standards, serial data communication interface standards, EIA-RS232 interface standard, RS-449, RS-422, RS-423 and RS-485 standards, Troubleshooting and testing with RS-485, GPIB standard, USB interface.

Error Detection, Cabling and Electrical Noise: Errors, Types of error detection, control and correction, copper and fiber cables, sources of electrical noise, shielding, cable ducting and earthling.

Modems and Multiplexers: Synchronous and Asynchronous modes, flow control, modulation techniques, types of a modem, modem standards, terminal and statistical multiplexers.

Communication Protocols: Flow control protocols, XON/XOFF, BSC, HDLC and File transfer protocols, OSI model and layers, ASCII protocols, Modbus protocol.

Industrial Protocols: Introduction to HART protocol, Smart instrumentation, HART physical layer, HART data link layer, HART application layer, ASD_i interface, Seriplex, CANbus, Device net, Profibus, FIP bus, Fieldbus.

Local Area Networks: Circuit and packet switching, Network topologies, Media access control mechanisms, LAN standards, Ethernet protocol, Token ring protocol.

References & Web Resources:

1. Practical data communications for instrumentation and control, John Park, Steve Mackay, Edwin Wright, Elsevier Newnes Publisher, 2008.
2. Computer Networks,Andrew Tanenbaum, Prentice Hall Professional Technical Reference, 2002.

CourseTitle	CourseCode	Structure (I-P-C)		
Design of Switched Mode Power Supplies		**3**	**0**	**3**

Pre-requisite, if any: Basic Electrical and Electronics Engg., and Control System

Course Outcomes: At the end of the course, the students will be able to:

CO1	Able to do the Steady-State Analysis of DC-DC power converters
CO2	Design switched-mode DC-DC power converters
CO3	Apply corresponding control techniques
CO4	Design transformer and different power sources for various DC-DC Applications
CO5	Demonstrate proficiency with computer skills (e.g., PSPICE and MATLAB) for the analysis and design of switched mode power converters.

Syllabus:

Switching devices: Ideal and real characteristics, control, drive and protection.

Design constraints of reactive elements in Power Electronic Systems: Design of inductor, transformer and capacitors for power electronic applications, Input filter requirement.

Switching power converters: Circuit topology, operation, steady-state model, dynamic model. PWM DC - DC Converters (CCM and DCM) - operating principles, constituent elements, characteristics, comparisons and selection criteria.

Soft-switching DC - DC Converters: Zero-voltage-switching converters, zero-current switching converters, multi-resonant converters and Load resonant converters.

Pulse Width Modulated Rectifiers: Properties of ideal rectifier, realization of near ideal rectifier, control of the current waveform, single phase and three-phase converter systems incorporating ideal rectifiers and design examples.

Review of linear control theory. Closed-loop control of switching power converters. Sample designs and construction projects.

Text Books:

1. R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd Kluwer Academic Publishers, 2000. ed.,

References:

1. Marian K. Kazimierczuk, ‘Pulse-width Modulated DC-DC Power Converters’ John Wiley & Sons Ltd., 1st Edition, 2008.

2. Philip T Krein, ‘Elements of Power Electronics’, Oxford University Press, 2nd Edition, 2012.

3. Batarseh, ‘Power Electronic Circuits’, John Wiley, 2nd Edition, 2004.

4. H. W. Whittington, B. W. Flynn, D. E. Macpherson, ‘Switched Mode Power Supplies’, John Wiley & Sons Inc., 2nd Edition, 1997.

Course Title	Course Code	Structure (I-P-C)		
Detection and Estimation Theory		**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Random Process, Communication Systems

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the discrete-time and continuous-time signal theory for finding unknown signal parameters.
CO2	Extract useful information from random observations in communications.
CO3	Design and analyze optimum detection schemes.
CO4	Estimate the error in wireless communication.
CO5	Understand the performance parameters in practical applications

Syllabus:

Detection Theory: Detection Theory in Signal Processing; the Detection Problem; the Mathematical Detection Problem; Hierarchy of Detection Problems; Role of Asymptotics.

Statistical Detection Theory: Neyman-Pearson Theorem , Receiver Operating Characteristics, Minimum Probability of Error, Multiple Hypothesis Testing, Minimum Bayes Risk Detector - Binary Hypothesis.

Deterministic Signal: Matched Filters – Development of Detector, Performance of Matched Filter; Multiple Signals – Binary case, Performance of Binary Case, M-ary case.

Random Signals: Estimator-Correlator – Energy Detector; Linear Model - Rayleigh Fading Sinusoid, Incoherent FSK for a Multipath Channel.

Estimation Theory: Estimation in Signal Processing; Mathematical Estimation Problem; Assessing Estimator Performance.

Minimum Variance Unbiased Estimation: Unbiased Estimators; Minimum Variance Criterion; Existence of the Minimum Variance Unbiased Estimator; Finding the Minimum Variance Unbiased Estimator. Estimator Accuracy Considerations; Cramer-Rao Lower Bound; General CRLB for Signals in AWGN.

Estimation Techniques: Linear Model, General Minimum Variance Unbiased Estimation, Best Linear Unbiased Estimators, Maximum Likelihood Estimation, Least Squares, Estimation.

Text Book(s):

1. Steven M. Kay, Fundamentals of Statistical signal processing, volume-1: Estimation theory. Prentice Hall 2011.
2. Steven M. Kay, Fundamentals of Statistical signal processing, volume-2: Detection theory, Prentice Hall 2011.

References & Web Resources:

1. Harry L. Van Trees, Detection, Estimation, and Modulation Theory, Part I, John Wiley & Sons, Inc. 2011.
2. A. Papoulis and S. Unnikrishna Pillai, Probability, Random Variables and stochastic processes, 4e. The McGraw-Hill 2010.

Course Title	Course Code	Structure (I-P-C)		
Digital Image Processing		**3**	**2**	**4**

Pre-requisite, if any: Digital Signal Processing

Course Outcomes: At the end of the course, the students will be able to:

CO1	Analyse the properties of various images
CO2	Manipulate the operations between the images
CO3	Transform the given images
CO4	Detect the objects in the images
CO5	Enhance the resolution of the images

Syllabus:

Theory

1. Digital Image Fundamentals: elements of visual perception, image acquisition and display, image sampling and quantization, pixel relationship, arithmetic operations between images and super resolution (4 hours)

2. Image Transformation and Enhancement: geometric transformation, intensity transformation, spatial domain filtering, DFT, DCT, KLT and frequency domain filtering (8 hours)

3. Image and Video coding: run length coding, Huffman coding, compression using DCT, H.264/MPEG-4 advanced video coding (4 hours)

4. Image Restoration and Reconstruction: models for image degradation and restoration process, Wieners' filter, principles of Computed Tomography (CT), Image reconstruction from projections using inverse Radon transform and binary image reconstruction using network flow (6 hours)

5. Color Image Processing: color models, pseudo and full-color image processing, smoothing and sharpening in color images and segmentation based on color (4 hours)

6. Morphological Image Processing: erosion and dilation, opening and closing, boundary extraction, hole filling, connected component extraction, thinning and thickening, and grayscale morphology (6 hours)

7. Image Segmentation: point, line and edge detection, Hough transform, thresholding using Otsu's method, region based segmentation, watershed segmentation algorithm and graph-cut based segmentation (7 hours)

8. Representation, Description and Recognition of Objects: chain codes, polygonal approximation approaches, signatures, boundary segments, boundary descriptors, regional descriptors, recognition based on decision–theoretic methods, matching shape numbers and string matching (7 hours)

Text Book(s):

1. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson Education, 3rd Edition, 2009

References & Web Resources:

1. William K Pratt, "Digital Image Processing", John Willey, 4th edition, 2006.
2. A.K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 1995.
3. Rafael C. Gonzalez, Richard E. Woods, and Steven L. Eddins, "Digital Image Processing using MATLAB", Pearson Education, 2nd Edition, 2009.
4. B. Chanda and D. Dutta Majumder, "Digital Image Processing and Analysis", Prentice Hall of India, 2008

CourseTitle	CourseCode	Structure(I-P-C)		
Electrical Drives		**1**	**3**	**3**

Pre-requisite,ifany: BasicElectricalandElectronicsEngineering

CourseOutcomes: Atthe endofthe course,thestudentswillbeableto:

CO1	Understandhowpowerelectronicconvertersandinvertersoperate.
CO2	Possessanunderstandingoffeedbackcontroltheory.
CO3	Analyze andcomparetheperformanceofDCandACmachines.
CO4	Designcontrolalgorithmsforelectricdriveswhichachievetheregulation oftorque, speed,or position inthe abovemachines.

Syllabus:

Experiments conducted in this course bring out the basic concepts of different types ofelectricalmachinesand theirperformance.

Experimentsareconductedtointroducetheconceptofcontrolofconventionalelectri cmotors such as DC motor, AC Induction motor and also special machines such as Steppermotor, Permanentmagnetbrushless motors,Servo motor.

Speed-Torquecharacteristicsofvarious typesofloadanddrivemotors arealsodiscussed.

The working principle of various power electronic converters is also studied by conductingexperiments.

References & Web Resources:

1. R.Krishnan,“ElectricMotorDrives:Modeling,Analysis,andControl,”Pre nticeHall, 2001.
2. .Mohan,“ElectricDrives:AnIntegrativeApproach,”MNPERE,2001.

Course Title	Course Code	Structure (I-P-C)		
Electromagnetic Interference and Compatibility		**3**	**0**	**3**

Pre-requisite, if any: Electromagnetic Waves and Transmission Lines

Course Outcomes: At the end of the course, the students will be able to:

CO1	Gain knowledge to understand the concept of EMI / EMC related to product design.
CO2	Understand the various standards of EMI/EMC.
CO3	Diagnose and solve various electromagnetic compatibility problems.
CO4	Understand the sources of EMI and various coupling methods.
CO5	Learn the various methods of doing the pre-compliance measurement techniques.

Syllabus:

Introduction to EMI and EMC: Various EMC requirements and standards-Need for EMC and its importance in electronic product design - sources of EMI - few case studies on EMC.

Conducted and radiated emission: power supply line filters-common mode and differential mode current-common mode choke-switched mode power supplies.

Shielding techniques: shielding effectiveness-shield behaviour for the electric and magnetic field - aperture-seams-conductive gaskets- conductive coatings.

Grounding techniques: signal ground-single point and multi-point grounding-system ground common impedance coupling -common mode choke-Digital circuit power distribution and grounding.

Contact protection: arc and glow discharge-contact protection network for inductive loads-C, RC, RCD protection circuit- inductive kickback.

RF and transient immunity: transient protection network- RFI mitigation filter-power line disturbance- ESD- human body model- ESD protection in system design.

PCB design for EMC compliance: PCB layout and stack up- multi-layerPCB objectives Return path discontinuities-mixed signal PCB layout.

EMC pre-compliance measurement: conducted and radiated emission test-LISN- Anechoic chamber.

Text Book(s):

1. H. W. Ott, Electromagnetic Compatibility Engineering, 2nd edition, John Wiley & Sons, 2011, ISBN: 9781118210659.
2. C. R. Paul, Introduction to Electromagnetic Compatibility, 2nd edition, Wiley India, 2010, ISBN: 9788126528752.

References & Web Resources:

1. K. L. Kaiser, Electromagnetic Compatibility Handbook, 1st edition, CRC Press, 2005. ISBN: 9780849320873.

Course Title	Course Code	Structure (I-P-C)		
MIMO Communication Systems		**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital Communications, and Wireless Communication.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concept of MIMO communication techniques, Channel Capacity, MIMO algorithms.
CO2	Understand power allocation strategies for practical MIMO systems.
CO3	Design algorithms of MIMO to improve the bit rate.
CO4	Understand MIMO in 5G communication.
CO5	Understand the MIMO reception in various channel conditions

Syllabus:

Introduction: Diversity-multiplexing trade-off, transmit diversity schemes, advantages and applications of MIMO systems.

Analytical MIMO channel models: Uncorrelated, fully correlated, separately correlated and keyhole MIMO fading models, parallel decomposition of MIMO channel.

Power allocation in MIMO systems:Uniform, adaptive and near optimal power allocation.

MIMO channel capacity: Capacity for deterministic and random MIMO channels, Capacity of i.i.d., separately correlated and keyhole Rayleigh fading MIMO channels.

Space-Time codes: Advantages, code design criteria, Alamouti space-time codes, SER analysis of Alamouti space-time code over fading channels, Space-time block codes, Space-time trellis codes, Performance analysis of Space-time codes over separately correlated MIMO channel, Space-time turbo codes.

MIMO detection: ML, ZF, MMSE, ZF-SIC, MMSE-SIC, LR based detection.

Advances in MIMO wireless communications: Spatial modulation, MIMO based cooperative communication and cognitive radio, multiuser MIMO, cognitive-femtocells and large MIMO systems for 5G wireless.

Text Book(s):

1. R. S. Kshetrimayum, Fundamentals of MIMO Wireless Communications, Cambridge University Press, 2017.
2. A. Chokhalingam and B. S. Rajan, Large MIMO systems, Cambridge University Press, 2014.

References & Web Resources:

1. B. Kumbhani and R. S. Kshetrimayum, MIMO Wireless Communications over Generalized Fading Channels, CRC Press, 2017
2. T. L. Marzetta, E. G. Larsson, H. Yang and H. Q. Ngo, Fundamentals of Massive
3. MIMO, Cambridge University Press, 2016.

Course Title	Course Code	Structure (I-P-C)

Numerical Techniques in Electromagnetics		3	0	3

Pre-requisite, if any: Electromagnetic Waves and Transmission Lines

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand how to computational solve different structures using Maxwell equations.
CO2	Understand various computational techniques and their pros and cons.
CO3	Understand which software works best in terms of speed, and accuracy for analysing a given structure
CO4	Develop codes to analyze the EM structures.
CO5	Gain knowledge need to develop EM simulation software tools

Syllabus:

Review of vector calculus, Overview of computational electromagnetics, Review of Maxwell's equations.
Analytical techniques in Electromagnetics.
Finite Difference Time Domain methods: Analysis, convergence, accuracy and numerical dispersion, incorporating dielectric and dispersive materials, absorbing boundary conditions, perfectly matched layers (PML), sources.

Moment Methods: Integral equations (EFIE,MFIE), Green's Functions, MOM.

Finite element methods: Formulation and Absorbing boundary conditions (FEM).

Applications of computational electromagnetic: Specific Absorption Rate, Radar RCS, Periodic structures, Eddy current calculations, capacitance and inductance calculations, Microwave inverse imaging, Antenna radiation problems, Calculating the modes of a waveguide structure using the integral equation method.

Text Book(s):

1. Numerical Techniques in Electromagnetic, Second Edition Hardcover – Import, 12 July 2000, by Matthew N.O. Sadiku
2. Analytical and Computational Methods in Electromagnetic, Artech House Electromagnetic Analysis, 30 September 2008, by Ramesh Garg, Raj Mittra

References & Web Resources:

1. Computational Electromagnetics for RF and Microwave Engineering, 28 October 2010, by David B. Davidson
2. Advanced Engineering Electromagnetics Paperback - 8 October 2008, by Constantine A. Balanis
3. Computational Methods for Electromagnetics: 4 (IEEE Press Series on Electromagnetic Wave Theory) Hardcover – Import, 12 December 1997, by Andrew F. Peterson, Scott L. Ray, Raj Mittra

CourseTitle	CourseCode	Structure(I-P-C)		
PowerElectronics		**3**	**0**	**3**

Pre-requisite,ifany: Electronic Devices

CourseOutcomes: Atthe endofthe course,thestudentswillbeableto:

CO1	Understand basic operation of various power semiconductor devices andpassive components
CO2	Understandthebasicprinciple ofswitchingcircuits.
CO3	DesignAC/DCrectifier,DC/DCconverterandDC/ACinvertercircuits.
CO4	Understandtherolepowerelectronicsplayintheimprovementofenergyusage,efficiencyandthedevelopmentofrenewableenergytechnologies.
CO5	Design different power converters

Syllabus:

Introduction topowerelectronics; applicationsandroleofpowerelectronics.

Introductiontopowersemiconductordevices,operatingcharacteristicsofPowerDiode,SCR,Power BJT, PowerMOSFET andIGBT;DrivercircuitsandSnubbercircuits.

Introduction to AC/DC rectifiers, principle of operation of phase controlled rectifiers, singlephaseandthreephaseAC-DClinecommutatedconverters,dualconverter,andintroductiontounitypowerfactorconverters. Applications: DCmotordrivesandBattery chargers.

Introduction to DC/DC converters, Principle of operation of DC/DC (Buck, Boost, Buck-Boost, Cuk, Fly-back and Forward) converters. Applications: Power supply, DC motor drivesand SMPS.

Introductionto DC/AC inverters, PWMtechniques, Principleof operationof single phaseand three phase DC-AC inverters, Applications: AC motor drives, UPS, active filters, CFL,renewable power generation,inductionanddielectricheating.

Text Book:

1. N.Mohan,T.Undeland,andW.Robbins,“PowerElectronics:Converters,Applications, andDesign,”3rdEdition,Wiley,2003.
2. M.Rashid,“PowerElectronics:Circuits,Devices&Applications,”Prentice Hall,3rdEdition,2003.

References & Web Resources:

1. J.P.Agrawal,“PowerElectronic Systems:TheoryandDesign,”Pearson,2013.
2. Batarseh,“PowerElectronicCircuits,”JohnWiley,2004.2.R.W.EricksonandD.Maksimovic,“Fundamentals ofPowerElectronics,”2ndEdition,Springer,2001.
3. R.W.EricksonandD.Maksimovic,“FundamentalsofPowerElectronics,” 2ndEdition,Springer,2001.

Course Title	Course Code	Structure (I-P-C)		
Reliable Digital Communication System Design		**3**	**0**	**3**

Pre-requisite, if any: Communication Systems, Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Learn the functional behaviour of various cryptography, intrusion detection, and error correction algorithms.
CO2	Learn to develop hardware architectures of various cryptography, intrusion detection, and error correction algorithms.
CO3	Develop the countermeasure prototypes of adversary attacks
CO4	Develop the crypto co-processors using FPGA.
CO5	Understand the algorithms of cryptography.

Syllabus:

Information theory, Entropy, Properties of Entropy

Goals of Relilable Digital Communication: first level of defense (integrity, confidentiality, authenticity, and availability) and second level of defense (resilience to attacks).

Galois Field Arithmetic: Introduction to Group, Ring, and Fields, Prime/Polynomial field representation, Irreducible polynomial, primitive polynomial, minimal polynomial, Galois field addition, LSB first/MSB first/Montgomery Galois field multiplication architectures-bit serial, bit parallel, digit serial, systolic, and scalable architectures, Modular exponentiators-Square-multiply algorithm and Montgomery Ladder algorithm, Extended Euclidean algorithm/Fermat's little theorem based multiplicative inverse architectures.

Symmetric Encryption/Decryption Architectures: DES, 3-DES, and AES (fully folded, parameterized parallel, and fully parallel architectures).

Asymmetric Encryption/Decryption Architectures: ECC (right-to-left, left-to-right, Montgomery based scalar multiplication in affine/projective co-ordinates) and RSA.

HASH architectures: SHA512 and SHA3.

Key exchange protocols: Diffie Helmen, Elgamal, Neuro crypto key exchange protocol.

Authentication schemes: Yang Shieh and EijiOkamato.

Pseudo random number generators, Stream ciphers.

Physical unclonable functions: RO PUF, larger decoder memory based PUF, and XOR PUF.

Intrusion Detection: Universal HASH functions, Cuckoo hashing, and Bloom filter.

Error detection codes: CRC, LRC, and parity check, Error correction codes-Hamming, BCH, Reed Solomon, LDPC, Convolutional, Turbo product, and concatenated codes,
Hardware/software co-design analogous between ASIC/FPGA/hardware-software co-designs, need for crypto accelerators (or coprocessors), and hardware/software partitioning based AES/ECC architectures.

Side channel analysis: Power attack, Bit masking, and Cache template attack.

Text Book(s):

1. Doug R. Stinson , Cryptography Theory and Practice, Third Edition, CRC Press, 2006.
2. Shu Lin and Daniel J Castello, Error Control Coding, Second Edition, Printice Hall, 2004.
3. Haykin, An Introduction to Analog and Digital Communications, wiley Vol 2, 2008.

References & Web Resources:

1. A. J. Menezes, P. C. van Oorshot, and S. A. Vanstone, Handbook of Applied Cryptography, CRC Press, 1996.
2. Jonathan Katz and Yehuda Lindell, Introduction to Modern Cryptography, CRC Press, 2015.
3. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, Hardware Security: Design, Threats and Safeguards, CRC Press, 2014.

Course Title	Course Code	Structure (I-P-C)		
RF and Microwave Integrated Circuits		**3**	**0**	**3**

Pre-requisite, if any: Electromagnetic Waves and Transmission Lines,and Analog Electronics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the differences in designing low frequency ICs, RFICs, and MMICs.
CO2	Analyse high frequency filters, couplers, amplifier, oscillators and mixer circuits.
CO3	Design high frequency filters, couplers, amplifiers.
CO4	Develop RFICs.
CO5	Develop MMICs.

Syllabus:

Electromagnetic Theory Review: Maxwell's Equations, Fields in Media and Boundary Conditions, The Wave Equation, General Plane Wave Solutions, Energy and Power, Transmission lines and waveguide solutions.

Transmission Line Theory: The Lumped-Element Circuit Model for a Transmission Line, Field Analysis of Transmission Lines, The Terminated Lossless Transmission Line, The Smith Chart, The Quarter-Wave Transformer, Generator and Load Mismatches, Lossy Transmission Lines, Transients on Transmission Lines.

Microwave Network Analysis: Impedance and Equivalent Voltages and Currents, Impedance and Admittance Matrices, The Scattering Matrix, The Transmission (ABCD) Matrix.

Impedance matching and tuning, Microwave filter design.

Noise and nonlinear distortion, active rf and microwave devices.

Microwave Power Amplifier, Low Noise Amplifier, Oscillator and Mixer Design.

Introduction to microwave systems.

Text Book(s):

1. David M Pozar, Microwave Engineering, 4th Edition, Wiley, 2013.
2. Behzad Razavi, RF Microelectronics, 2nd Edition, Pearson, 2011.

References & Web Resources:

1. Robert E Collin, Foundations for Microwave Engineering, 2nd Edition, Wiley, 2007.
2. I.D. Robertson , S. Lucyszyn, RFIC and MMIC Design and Technology: 13 (Materials, Circuits and Devices), Institution of Engineering and Technology, 2001.

Course Title	Course Code	Structure (I-P-C)		
Satellite Communication		**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the satellite communication.
CO2	Understand the orbits and space of satellite communication.
CO3	Understand the optical communication.
CO4	Develop the packet switched networks.
CO5	Understand the importance of Optical technology in space applications

Syllabus:

OVERVIEW OF SATELLITE SYSTEMS, ORBITS AND LAUNCHING METHODS: Introduction, Frequency Allocations for Satellite Services, Intelsat, U. S. Domsats Polar Orbiting Satellites, Problems, Kepler's First Law, Kepler's Second Law, Kepler's Third Law, Definitions of Terms for Earth-orbiting Satellites, Orbital Elements, Apogee and Perigee Heights, Orbital Perturbations, Effects of a Non-spherical Earth, Atmospheric Drag, Inclined Orbits, Calendars, Universal Time, Julian Dates, Sidereal Time, The Orbital Plane, The Geocentric, Equatorial Coordinate System, Earth Station Referred to the IJK Frame, The Top centric-Horizon Co-ordinate System, The Sub-satellite Point, Predicting Satellite Position.

GEOSTATIONARY ORBIT & SPACE SEGMENT: Introduction, Antenna Look Angels, The Polar Mount Antenna , Limits of Visibility , Near Geostationary Orbits, Earth Eclipse of Satellite, Sun Transit Outage, Launching Orbits, Problems, Power Supply, Attitude Control, Spinning Satellite Stabilization, Momentum Wheel Stabilization, Station Keeping, Thermal Control, TT&C Subsystem , Transponders, Wideband Receiver, Input De-multiplexer, Power Amplifier, Antenna Subsystem, Morelos, Anik-E, Advanced Tiros-N Spacecraft.

OPTICAL NETWORK ARCHITECTURES: Introduction to Optical Networks; Layered Architecture- Spectrum partitioning, Network Nodes, Network Access Stations, Overlay Processor, Logical network overlays, Connection Management and Control; Static and Wavelength Routed Networks; Linear Light wave networks; Logically Routed Networks; Traffic Grooming; The Optical Control Plane- Architecture, Interfaces, Functions; Generalized Multiprotocol Label Switching – MPLS network and protocol stack, Link management, Routing and Signaling in GMPLS.

OPTICAL PACKET SWITCHED NETWORKS: Network Architectures- Unbuffered Networks, Buffering Strategies; OPS enabling technologies, Test beds; Optical Burst Switching, Switching protocols, Contention Resolution, Optical Label Switching, OLS network test beds, Control and Management – Network management functions, Configuration management, Performance management, Fault management, Optical safety, Service interface; network Survivability- Protection in SONET / SDH and IP Networks, Optical layer Protection, Interworking between layers.

FREE SPACE OPTICAL COMMUNICATION: Analog and digital FSOC data link, atmospheric attenuation, scattering, scintillation index, beam wandering, beam wave front aberration, adaptive optics, active optics, deformable mirror control, RoFSO, atmospheric channel models, estimation of refractive index, modulation and demodulation techniques, error control techniques.

Text Book(s):

1. Satellite Communications, Dennis Roddy, McGraw-Hill Publication Third edition2001
2. Satellite Communications – Timothy Pratt, Charles Bostian and Jeremy Allnutt, WSE, Wiley Publications, 2nd Edition, 2003.

References & Web Resources:

1. Timothy Pratt – Charles Bostian& Jeremy Allmuti, Satellite Communications, John Willy & Sons (Asia) Pvt. Ltd. 2004
2. Wilbur L. Pritchars Henri G. SuyderHond Robert A. Nelson, Satellite Communication Systems Engineering, Pearson Education Ltd., Second edition 2003.
3. Satellite Communications: Design Principles – M. Richharia, BS Publications, 2nd Edition, 2003.
4. J. Gower, "Optical Communication System", Prentice Hall of India, 2001
5. Rajiv Ramaswami, "Optical Networks ", Second Edition, Elsevier, 2004.
6. Satellite Communications Engineering – Wilbur L. Pritchard, Robert A Nelson and Henri G. Suyderhoud, 2nd Edition, Pearson Publications, 2003.
7. Optical Fiber Communication – John M. Senior – Pearson Education – Second Edition. 2007
8. Optical Fiber Communication – Gerd Keiser – McGraw Hill – Third Edition. 2000

CourseTitle	CourseCode	Structure(I-P-C)		
Sensing and Instrumentation		**1**	**3**	**3**

Pre-requisite, if any: Nil

CourseOutcomes: Atthe endofthe course,thestudentswillbeableto:

CO1	Buildsystemswhichwouldsensethedifferentphysicalsignal
CO2	Processthesignalsintherequiredanalogordigitalformats
CO3	Calibratesensorsaccordingtherequiredapplications.
CO4	Understandthecharacteristicsoftransducers.

Syllabus:

Transducers, transducer sensing and functions, Passive and active – Resistance, inductanceand capacitance,Strain Gauges, Hall Effect sensors, Opticalsensors.

Measurementofnon-electricalquantitiessuchasdisplacement,velocity,acceleration,pressure, force, flow and temperature, calibration of sensors, Data acquisition and detectiontechniques, Signalconversion, PC-based Instrumentation System.

Practiceincludesexperimentsfromfollowingtopics:

Signal generation – Instrumentation amplifiers – Signal conversion and processing –CharacteristicsofTransducers-Calibrationofsensors–Measurementofphysicalquantities.

Text Book(s):

1. AlanS.Morris,MeasurementandInstrumentationPrinciples,Elsevier,2001.
2. Sawhney. A. K, Course in Electrical & Electronics Measurement &Instrumentation, DhanpatRai, 2007.

References & Web Resources:

1. Howard Austerlitz,Dataacquisitiontechniquesusing PCs, AcademicPress, 2ndEd.2002.
2. BruceMihura,LabVIEWforDataAcquisition(NationalInstrumentsVirtualInstrumentation Series), PrenticeHall,2001.

CourseTitle	CourseCode	Structure(I-P-C)		
Signal and Power Integrity		**3**	**0**	**3**

Pre-requisite, if any: Nil

CourseOutcomes: Atthe endofthe course,thestudentswillbeableto:

CO1	Understand the design guidelines to be followed in PCB design and IC packagingto prevent Signal and Power Integrity issues.
CO2	Analyze the physical structure and dimensions of the PCB elements and fit an appropriate circuit model.
CO3	Analyze the measured voltages and currents in the PCB and find the causes of the signal integrity issues.
CO4	Analyze the measured voltages and currents in the PCB and find the causes of the power integrity issues.
CO5	Design an optimal layout for a PCB to avoid signal and power integrity issues.

Syllabus:
Signal Integrity Is in Your Future: What Are Signal Integrity, Power Integrity, and Electromagnetic Compatibility?, Signal-Integrity Effects on One Net, Cross Talk, Rail-Collapse Noise, Electromagnetic Interference (EMI, Two Important Signal-Integrity Generalizations, Trends in Electronic Products, The Need for a New Design Methodology, A New Product Design Methodology.

Time and Frequency Domains: The Time Domain, Sine Waves in the Frequency Domain, Shorter Time to a Solution in the Frequency Domain, Sine-Wave Features, The Spectrum of a Repetitive Signal, The Spectrum of an Ideal Square Wave, Frequency Domain to the Time Domain, Effect of Bandwidth on Rise Time, Bandwidth and Rise Time, Bandwidth of Real Signals, Bandwidth and Clock Frequency, Bandwidth of a Measurement, Bandwidth of a Model, Bandwidth of an Interconnect.

Impedance and Electrical Models, The Physical Basis of Resistance, Capacitance, Inductance, and Transmissions lines.

Transmission Lines and Reflections, Lossy Lines, Rise-Time Degradation, and Material Properties, Cross Talk in Transmission Lines.

Differential Pairs and Differential Impedance, S-Parameters for Signal-Integrity Applications, The Power Distribution Network (PDN)

Text Book(s):

1. Bogatin, Eric. Signal and power integrity-simplified. Pearson Education, 2010.

References & Web Resources:

1. Johnson, Howard, Howard W. Johnson, and Martin Graham. High-speed signal propagation: advanced black magic. Prentice Hall Professional, 2003.
2. Johnson, Howard W., and Martin Graham. High-speed digital design: a handbook of black magic. Vol. 155. Englewood Cliffs, NJ: Prentice Hall, 1993.

Course Title	Course Code	Structure (I-P-C)		
Software Defined Radio		**3**	**0**	**3**

Pre-requisite, if any: Signals and Systems, Analog and Digital, Wireless Communication Techniques.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the SDR, CR, and their applications.
CO2	Understand the signal processing architectures used in the SDR.
CO3	Develop the FPGA based SDR.
CO4	Develop microcontroller based SDR.

Syllabus:

INTRODUCTION TO SDR: What is Software-Defined Radio, The Requirement for Software-Defined Radio, Legacy Systems, The Benefits of Multi-standard Terminals, Economies of Scale, Global Roaming, Service Upgrading, Adaptive Modulation and Coding, Operational Requirements, Key Requirements, Reconfiguration Mechanisms, , Handset Model, New Base-Station and Network, Architectures, Separation of Digital and RF, Tower-Top Mounting, BTS Hoteling, Smart Antenna Systems, Smart Antenna System Architectures, Power Consumption Issues, Calibration Issues, Projects and Sources of Information on Software Defined Radio.

BASIC ARCHITECTURE OF A SOFTWARE DEFINED RADIO: Software Defined Radio Architectures, Ideal Software Defined Radio Architecture, Required Hardware Specifications, Digital Aspects of a Software Defined Radio, Digital Hardware, Alternative Digital Processing Options for BTS Applications, Alternative Digital Processing Options for Handset Applications, Current Technology Limitations, A/D Signal-to-Noise Ratio and Power 343 Consumption, Derivation of Minimum Power Consumption, Power Consumption Examples, ADC Performance Trends, Impact of Superconducting Technologies on Future SDR Systems.

SIGNAL PROCESSING DEVICES AND ARCHITECTURES: General Purpose Processors, Digital Signal Processors, Field Programmable Gate Arrays, Specialized Processing Units, Tilera Tile Processor, Application-Specific Integrated Circuits, Hybrid Solutions, Choosing a DSP Solution. GPP-Based SDR, Non real time Radios, High-Throughput GPP-Based SDR, FPGA-Based SDR, Separate Configurations, Multi-Waveform Configuration, Partial Reconfiguration, Host Interface, Memory-Mapped Interface to Hardware, Packet Interface, Architecture for FPGA-Based SDR, Configuration, Data Flow, Advanced Bus Architectures, Parallelizing for Higher Throughput, Hybrid and Multi-FPGA Architectures, Hardware Acceleration, Software Considerations, Multiple HA and Resource Sharing, Multi-Channel SDR.

COGNITIVE RADIO : TECHNIQUES AND SIGNAL PROCESSING:History and background, Communication policy and Spectrum Management, Cognitive radio cycle, Cognitive radio architecture, SDR architecture for cognitive radio, Spectrum sensing Single node sensing: energy detection, cyclostationary and wavelet based sensing- problem formulation and performance analysis based on probability of detection vs SNR. Cooperative sensing: different fusion rules, wideband spectrum sensing- problem formulation and performance analysis based on probability of detection vs SNR.

COGNITIVE RADIO: HARDWARE AND APPLICATIONS: Spectrum allocation models. Spectrum handoff, Cognitive radio performance analysis. Hardware platforms for Cognitive radio (USRP, WARP), details of USRP board, Applications of Cognitive radio.

Text Book(s):

1. "RF and Baseband Techniques for Software Defined Radio" Peter B. Kenington, ARTECH HOUSE, INC © 2005.
2. "Implementing Software Defined Radio", Eugene Grayver, Springer, New York Heidelberg Dordrecht London, ISBN 978-1-4419-9332-8 (eBook) 2013.

References & Web Resources:

1. "Cognitive Radio Technology", by Bruce A. Fette, Elsevier, ISBN 10: 0-7506-7952-2, 2006.
2. "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", Hüseyin Arslan, Springer, ISBN 978-1-4020-5541-6 (HB), 2007.

Course Title	Course Code	Structure (I-P-C)		
Testing and Testability		**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Syllabus:

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models.

Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods.

Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Fault Diagnosis Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

Text Book(s):

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990
2. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002

References & Web Resources:

1. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000
2. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
4. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
5. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
6. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International.

Course Title	Course Code	Structure (I-P-C)		
VLSI Technology		**3**	**2**	**4**

Pre-requisite, if any: Electronic Devices

Course Outcomes: At the end of the course, the students will be able to:

CO1	Appreciate the intricacies involved in VLSI circuit fabrication.
CO2	Understand the various processes needed to fabricate the VLSI devices.
CO3	Learn fabrication steps for existing and coming generation devices.

Syllabus:

Theory

1. Introduction to VLSI Design, Bipolar Junction Transistor Fabrication, MOSFET Fabrication. (3 hours)

2. Crystal Structure of Si, Defects in Crystal, Crystal growth (3 hours)

3. Epitaxy, Vapour phase Epitaxy, Doping during Epitaxy, Molecular beam Epitaxy (3 hours)

4. Oxidation – Kinetics, Rate constants, Dopant Redistribution, Oxide Charges (3 hours)

5. Diffusion-Theory of Diffusion, Doping Profiles, Diffusion Systems Ion Implantation - Process, Annealing of Damages, Masking during Implantation (3 hours)

6. Lithography, immersion lithography, e-beam lithography (3 hours)

7. Etching-Wet Chemical Etching, Dry Etching, Plasma Etching, Si, SiO2, SiN and other materials (3 hours)

8. Deposition-Plasma Deposition, Metallization, Problems in Aluminium Metal contacts, Copper interconnects (3 hours)

9. IC BJT - LOCOS, Trench isolation, Poly-emitter-poly-base-BJT and its suitability for high-speed applications (3 hours)

10. MOSFET - Metal gate vs. Self-aligned Poly-gate, Tailoring of Device Parameters, CMOS Technology, Latch - up in CMOS, MOSFET structures with strained channels and high-k gate dielectrics, Bi-CMOS Technology, introduction to FINFETs (3 hours)

11. Small-Dimension Effects of MOSFET: Modelling for Circuits Simulation- Quantum-Mechanical Effects; Gate Current, Junction Leakage, Scaling and New Technologies, Approaches, and Properties of Good Models, Model Formulation Considerations, Parameter Extraction, Compact Models, Benchmark Tests (7 hours)

12. Small-Signal Modelling of MOSFET: Conductance Parameter Definitions and Equivalent Circuits, Conductance Parameters Due to Gate and Body Leakage, Transconductance, Source-Drain and Output Conductance, Capacitance Definitions and Equivalent Circuits, Capacitance Evaluation and Properties, y-Parameter Model, RF Models (6 hours)

Practice

1. Simulation of various properties of Si, SiO2, SiN and other materials (40 hours)

Text Book(s):

1. S. K. Ghandhi, “VLSI Fabrication Principles- Silicon and Gallium Arsenide”, Wiley Publications.

2. Y. Tsividis and C. McAndrew, “MOSFET modelling for Circuit Simulation”, Oxford University Press, 2011

References & Web Resources:

1. S. M. Sze, “VLSI Technology”, Tata McGraw Hill, 2008

2. J. Plummer, M. D. Deal, and P. B. Griffin, “Silicon VLSI Technology, Fundamentals, Practice and Modeling”, Pearson Higher Education, 2000

3. T. A. Fjeldly, T. Yetterdal, and M. Shur, “Introduction to Device Modeling and Circuit Simulation”, John Wiley, 1998.

4. Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 1998.